

Realize Your Product Promise®

Modern Simulation Solutions for Signal and Power Integrity for Efficient Design of PCBs

Fluid Dynamics

Structural Mechanics

Electromagnetics

Systems and Multiphysics

Peter Krenz, Application Engineer



Introduction

- High Frequency Simulation Tools Overview

- Cannel Simulation Flow
- Slwave Capabilities
- Test case:
 - Decoupling Capacitor Optimization
 - PCI Express 8 GT/s Channel

• Summary



ANSYS: High Frequency Applications Overview



What is HFSS?

- Premier 3D Electromagnetic design tool
- Solves
 - Any arbitrary 3D structure
- Uses
 - Full Wave Finite Element Method (FEM)
 - Transient Finite Element Solver
 - Integral Equation Solver
 - Physical Optics Solver



Release v2014.0



- ANSYS SIwave evaluates designs from entire package, board, or package on board
- Slwave includes all effects of coupling between traces, packages, and board
 - Advanced Signal- and Power-Integrity Analysis
 - Easy Layout Extraction (S,Y,Z)
 - Automated Decoupling Capacitor Optimization
 - Integrated and Automated DC I²R Reporting
 - Advanced Broadband SPICE Model Generation
 - Highly Accurate Macro Modeling
 - High-Performance Computing
 - Comprehensive Multi-physics (Icepak)





- Integrates ANSYS HF tools into a seamless system simulation
- Solves
 - Time / frequency circuits and systems
- Uses
 - State Space or convolution time domain spice solver
 - Harmonic Balance frequency domain solver
 - 2D / 3D Method of Moment solver

• Applications

- Time and / or frequency domain circuit analysis
- Signal Integrity
- Antenna Arrays
- RF IC simulation



Release v2014.0



Slwave: Channel Simulation Flow

ANSYS Introduction: Channel Simulation Flow

Post layout validation Simulate the physical architectures, create electromagneticbased models, and apply time domain signaling in conjunction with these models.

ANSYS has streamlined this process for engineers with the use of one product: *Slwave*





- A pass/fail solution quickly shows engineers if their design is sufficient or not.
- ANSYS Solution Gold Standard Accuracy with Parasitic Extraction
- Each component of the channel can be decomposed, studied, and optimized
- This solution provides the Why

<u> </u>	
Design Details	
Description	
Project Design	PCIe Example PCIe Specification Test
Design ID	492
Design Type	Circuit Design
Location	D:/ANSYS/UGMStuff/ForBo
Date	10/3/2012 4:17:10 PM
Product Version	Designer 8.0.0
UDD Version	Design Summary, 1.0 (R14.5)
User	gbames





Slwave: Power and Signal Integrity Extractor



- ANSYS SIwave evaluates designs from entire package, board, or package on board
- Slwave includes all effects of coupling between traces, packages, and board
 - Advanced Signal- and Power-Integrity Analysis
 - Easy Layout Extraction (S,Y,Z)
 - Automated Decoupling Capacitor Optimization
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 - Advanced Broadband SPICE Model Generation
 - Highly Accurate Macro Modeling
 - High-Performance Computing
 - Comprehensive Multi-physics (Icepak)





Slwave: More Than 2.5D

<u>E</u> xport	Simulation Results Help
🏷 🖋 ⊴⊂ 🐢	SIwave Sentinel-PSI HFSS for ECAD
	PI Advisor PDN Channel Builder

- Slwave 2.5D Full wave Hybrid solver
- Slwave 2.5D Full wave Hybrid solver + Q3d
- HFSS 3D Full Wave FEM

weep	Sensitivity			
Fre	Simulation quency Range	SYZ Sv	veep 1	
	Start Freq	Stop Freq	Num. Points / Step Size	Distribution
1	0Hz	0Hz	1	Linear
2	1Hz	1MHz	25	By Decade
з	1MHz	15GHz	250	Linear
Swe	Discrete Swee	p Sween	Set FWS generation Min Rise/Fall T	ation parameters ïme / s
En	ror Tolerance	0.005	3.33333E-11	
			SIwave with 3D	DDM

ANSYS Full-Wave Package/Board Positioning

Arbitrary 3D



HFSS-Solver on Demand



SI

- Golden Accuracy Simulator
- Solves Any 3D geometry
- Powerful for Critical Nets
- Layout Front-end for HFSS

Any Geometry Gold Standard Accuracy

L1-0: 13 © 2014 ANSYS, Inc. November 18, 2014



Hybrid

Board + Package

Slwave

- FAST Hybrid method for PKG/BRD
- Marked ease of interaction with Complicated Board geometries
- Handles many, but not all 3D effects

SPEED



Slwave Includes Alinks for EDA

<u>F</u> ile	Edit View Draw Circuit Eleme	nts <u>T</u> ools 3D <u>E</u> xport <u>S</u> imulation <u>R</u> esults <u>H</u> elp	
0	New Ctrl+N	🗟 🍪 🖸 🐜 🏭 😕 🧭 🛛 VIA M1 M4	
2	Open Ctrl+O	Q +	
	Save As	→ ₽ ×	
	Run Script	acitors	
	Import •	ANF	X
	Export	AnsoftLinks <= 6.0 Project	
89	Launch SIwave™ Reporter	Apache CPM/PLOC File	
	<u>1</u> SIwave DC Analysis.siw <u>2</u> SIwave_brd_1.2.siw <u>3</u> C:\Users\\FGB_odb_v17.siw <u>4</u> C:\Users\\FGB_odb_v17.siw <u>5</u> SIwave_brd_1.2.siw	Component File Component Mapping File Huray Roughness Models Layer Stackup Plane Extents	wse wse
	<u>6</u> SIwave DC Analysis.siw <u>7</u> C:\Users\\EMI.siw	Mentor Board Station RE/X/ Design Mentor Expedition Design	
	<u>8</u> E70555_004_Test.siw	Mentor PADS Design	
	Exit	ODB++ Design Zuken CR5000 Design	Corr Corr
0: 1	4 © 2014 ANSYS, Inc. N	ovember 18, 2014	



Slwave: NEW DesignerSI Circuit Capability



Designer for SI



- Circuit Simulator- Nexxim Engine (transient, fast convolution, statistical and IBIS-AMI circuit simulation)
- Integrated Schematic capture and layout tool
- Design management front-end linking EM simulation products (HFSS, Q3D, SIwave, ..)
- 2D quasi-static field solver
- HFSS Solver on Demand



Nexxim Engine: Simulation Piece of Mind

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(Nexxim	C Designer System	C HSPICE
Int	erpolation	Linear	•
Ex	trapolation	Constant magnitude, linear phase	extrapolation 💌
D	Behavior	Constant magnitude, linear phase	extrapolation 💌
M	ethod	State Space Model	•
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at DC is needed for harmonic balance and n. select the behavior of this NPORT.	I transient analysis. If the data at
C Designer System	C HSPICE
Linear	•
Constant magnitude, linear ph	ase extrapolation 💌
Constant magnitude, linear ph	ase extrapolation 💌
State Space Model	•
State Space Model	
Convolution - Piecewise Linea	ar Transform
Convolution - Linear interpolati	ion of IFFT
ons	
	at DC is needed for harmonic balance and n, select the behavior of this NPORT.

Models extracted out from our electromagnetic solvers are handled correctly.

Nexxim engine can ensure that the models you run are causal and passive in the time domain.

Nexxim will enforce these criteria for outside models as well.

User can just click the option and go. There is no guess work!



- UDO (User Defined Outputs) allows calculations and post-processing of use raw transient simulation data
 - Designer SDF file
 - H-Spice TRO file

• Key benefits:

- Non-Ideal voltage supply is supported
- Every bit-by-bit falling and rising transition edge is calculated
- Fully customizable through Python scripts.
 - UDOs specific to LPDDR, DDR2 and DDR3 standards already exist!



What is an ANSYS UDO?





• Example of a potential report created in PDF and HTML format

١	/irtual Compliance Test	Table 2. Data Timing Res	alts - All DQ, All Edges (Sec 13.1)	Table 4.	AC and DC	Input Levels				
	intual compliance rest	Metric Worst Actual	Worst Margin Spec Value Unit Notes		AC and DC	Input Levels fo	r Single-Ended	Data Signals []	√] (Sec 8.1.2)	
		tDS(base) 252.256	242.256 10 ps	Vref		-	_			C
Table	of Contents	tDH(base) 87.370	42.370 45 ps	VIH(dc)						0
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Summary .	1	tDH(derated) 9.370	-35.629 45 ps	VIH(ac)						
Meas	auement Results 2	tDQSQ 94.661	5.338 100 ps t(worst)=56807.334ps	VIL(ac)						
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AC a	nd DC Input Levels	1.00	Curve Info	VIHdiff(ac) Min					
Per I	Q Metrics 3	131-	Record Terrare W/29Ubdes (0015000)	VIL.diff(ac) Max					
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Speed Grade Voltage Level Spee Version Project Design Variation Date Product Version Date	System Description DDR3-1600 AC150 AC150 IESD79-3E DR3_W_element_dynamic_link Start Summary Non-IP_DDR3_Example DDR3_W_element_dynamic_link SCPU_Conse_Index=""SPO_COST_Stomagh_Index="DIN_ODT_OFF" SDM_M_SDM_MARK_STOMAGHT_STOMAGH	Z and zero of the second secon	stion Configuration DDR3 AC-Timing 4-DQ1 Compare DDR3 AC Timing Margines for 4-DQ 1.08 Probes V(CPU Buffees1 U118.DQS, P) V(CPU Buffees1 U118.DQS, N) V(CPU Buffees1 U118.DQS) V(CPU Buffees1 U118.DQS) V(CPU Buffees1 U118.DQS) V(CPU Buffees1 U118.DQS) V(CPU Buffees1 U118.DQS) V(CPU Buffees1 U118.DQS) V(CPU Buffees1 U118.DQS)	Mean Freq Ski Deviati Per DQ Met Table 6. 1 2 3 tDS(base) 0 1 2 3 tDS(derati 0 1	vency out rrics Data Line M Min(ps) 263.883 252.256 261.886 262.872 Min(ps) 134.338 133.775 87.370 130.352 ed) Min(ps) 211.882 220.399	I601.53 22.249 Jackpol 434.121 437.673 436.666 438.075 Max[po] 225.145 225.135 225.132 217.446 212.312 Max[po] 317.885 316.673	8 Mean(ps] 379.195 378.660 378.670 Mean(ps] 174.711 173.092 171.894 Mean(ps] 171.894 Mean(ps) 276.570 278.284	BPS BPS BPS StdDer(pa) 47.872 50.574 50.128 49.825 StdDer(pa) 23.660 23.374 26.477 23.975 StdDer(pa) 27.843 27.843	t(worst)[p2] 57436.92 50560.82 49936.78 51187.68 27440.77 76189.79 2005.29 68072.95 ft(worst)[p2] 57436.91 57436.91 53700.90	Ma 253 242 251 252 Ma 89. 88. 85 85 Ma 201 210
Speed Grade Version Project Design Variation Date Product Version UDD Version	System Description DDR3-1600 AC150 AC150	Z and the second	tion Configuration DDR 3A-Timing 4-DQ1 Compare DDR3 AC Timing Margines for 4-DQ 1.08 Probes Void V(CPU Buffers1 U118DQ5_P) V(CPU Buffers1 U118DQ5_N) V(CPU Buffers1 U118DQ5_N) V(CPU Buffers1 U118DQ2) V(CPU Buffers1 U118DQ2)	Mean Freq Ski Deviati Per DQ Met Table 6.1 2 3 tDS(bare) 0 1 2 3 tDH(bare) 0 1 2 3 tDS(derati 0 1 2 3 tDS(derati	vency ion TriCS Data Line M Min(pa) 266.883 252.256 261.386 262.872 Min(pa) 134.338 134.338 134.338 134.338 134.338 232.870 201.882 201.88	I601.53 22.249 Idetrics Max[ps] 434.121 437.673 434.121 436.566 438.075 Max[ps] 225.145 212.312 121.245 317.685 316.673	8 Mean[ps] 379.195 378.690 378.670 Mean[ps] 174.711 173.092 172.594 Mean[ps] 276.570 278.244 Mean[ps] 276.570 278.284	BPS BPS BPS SteDev(ps) 47:872 50:574 50:128 49:825 SteDev(ps) 23:660 23:74 26:477 SteDev(ps) 23:75 SteDev(ps) 77:221 77:231 27:843 28:468	t(worst)[p2] 5736.92 49936.78 5137.86 (wwwst)[p2] 27440.77 76189.79 2505.29 (twwst)[p2] 57345.91 35300.90 49936.78	Ma 2533 242 251 252 Ma 89 85 85 Ma 201 210 198
Speed Grade Voltage Voltage Version Project Project Project Project Project Project Design Variation Date Product Version Date Version UDD Version UDD Version UDD Version UDD Version UDD	System Description DDR3-1600 AC150 AC150	T and the second	tion Configuration Perception Val V(CPU Berfinal UllBADQS_P) V(CPU Berfinal UllBADQS_P) V(CPU Berfinal UllBADQS_N) V(CPU Berlinal ULLBAD	Mean Freq Sol Deviat Per DQ Met Table 6. 1 US(base) 0 1 2 3 UBH(base) 0 1 2 3 US(derate 0 1 2 3 3 US(derate 0 1 2 3 3 US(derate 3 3 US(derate) 3 US(derate) 3 US(bas) 3 US(base)	vency ion TriCS Data Line M Min(pa) 263.883 252.256 261.386 261.386 262.872 Min(pa) 134.338 133.775 87.370 134.338 134.338 20.1386 20.0399 20.1386 20.1386 20.1386 20.1386 20.1389 20.1386 20.1486 20	I601.53 22.249 Mase[ps] 434.121 437.673 436.566 438.075 225.145 217.446 212.312 Mase[ps] 317.6873 316.673 317.673 318.075	8 Mean[ps] 379.195 378.690 379.595 378.470 Mean[ps] 174.711 173.092 172.598 171.894 Mean[ps] 276.570 278.284 277.281 277.294	BP5 BP5 StdDer(p2) 47.872 50.574 50.128 49.825 StdDer(p2) 23.660 25.374 26.477 23.975 StdDer(p2) 27.221 27.843 25.468 27.316	t(worst)[p2] 57436.92 50560.82 49936.78 51187.86 t(worst)[p2] 27440.77 76189.79 2505.29 68077.95 (worst)[p2] 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.91 57436.92 57757.95 5775757.95	Maa 253 242 251 252 89 88. 85 85 201 210 198 205
Speed Grade Voltage Level Spee Version Variation Location Date Product Version User	System Description DDR3-1600 AC150 AC150 IESD79-3E Test Summary Non-IP_DDR3_Example DDR3_V_element_dynamic_link DDR3_D_index="typ" SCPU_RX_ODT_Sneugh_index="DIN_ODT_OFF" SDImm_RDN_DModel: DDImm_RD_index="typ" SCPU_RX_ODT_Sneugh_index="Typ". SDImm_Conse_Index="typ". DDIM_SUB_Index="typ" SCPU_RX_ODT_Sneugh_index="Typ". SOS:ODM_VA="SMain_RDI_Index="typ". Clubooft ProjectV_UnualCompliance/Steve_IP_FREE_Example I22220118-47:14 AM 7.0 1.08 bboott: Index Index Index	Z and zero of the speed Bin	tion Configuration Description Description DBS AC Timing 4-DQ1 Compute DDS3 AC Timing Margines for 4-DQ 1.08 Probes Vdd V(CPU Buffen1/U118 DQ5, p) V(CPU Buffen1/U118 DQ5, N) V(CPU Buffen1/	Mean Freq Ski Devian Per DQ Met Table 6. 1 2 3 tDH(base) 0 1 2 3 3 tDH(base) 0 1 2 3 3 tDS(derah 0 1 2 3 3 tDS(derah 0 3 tDS(derah 1 3 3 tDS(derah 1 3 tDS(base) 1 3 tDS(base) 1 3 tDS(base) 1 1 3 tDS(base) 1 1 1 2 3 3 tDS(base) 1 1 1 2 3 3 tDS(base) 1 1 1 1 2 3 3 tDS(base) 1 1 1 1 2 3 3 tDS(base) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1	vency ion	1601.53 22.249 Mas(ps) 434.121 437.673 436.566 438.072 228.389 225.145 217.446 217.446 212.312 Mas(ps) 317.885 316.673 318.075 318.075 318.075	8 Mean[ps] 379.195 378.690 379.527 378.670 379.527 378.470 379.527 378.470 379.527 378.470 174.711 173.592 174.711 173.592 174.711 173.592 172.593 172.593 278.284 277.821 277.947 Mean[ps]	BP5 BP5 BP5 StdDer(pa) 47.872 50.574 50.128 49.825 StdDer(pa) 23.660 25.374 26.477 23.975 StdDer(pa) 27.221 27.843 28.486 27.316 StdDer(pa)	t(worst)[p2] 50560.82 49936.78 51187.86 127440.77 76189.79 27440.77 76189.79 2505.29 68072.95 4(worst)[p2] 57436.91 53700.90 49936.78 54319.08 t(worst)[p2]	Ma 253 242 251 255 Ma 89. 85. 85. Ma 201 210 198 205 Ma
Speed Grade Voltage Level Spee Version Variation Date Project Design Variation Date Version UDD Version User	System Description DDR3-1600 AC150 AC150 IESD79-3E DR3_W_element_dynamic_link Structure of the system	Z and the second	tion Configuration DDR3 AC Tuning 4-DQ1 Compare DDR3 AC Tuning Margines for 4-DQ 1.08 Probes V(CPU Batfiers1U118DQ5_P) V(CPU Batfiers1U118DQ5_P) V(CPU Batfiers1U118DQ5_N) V(CPU Batfiers1U118DQ2) V(CPU Batfiers1U1	Mean Freq Ski Deviati Per DQ Met Table 6.1 2 3 tDH(bace) 0 1 2 3 tDH(bace) 0 1 2 3 tDH(bace) 0 1 2 3 tDH(bace) 0 1 2 3 tDH(bace) 0 1 2 3 tDH(bace) 0 0 1 2 3 tDH(bace) 0 0 1 2 3 tDH(bace) 0 0 0 1 1 2 3 tDH(bace) 0 0 0 1 1 2 3 tDH(bace) 0 0 0 1 1 2 1 1 1 1 1 1 1 1 1 1 1 1 1 1	Venicy ion TriCS Nata Line M Minipa] 263,883 263,883 264,887 264,887 264,887 264,887 264,887 264,887 134,338 133,775 87,370 134,338 133,775 87,370 134,338 133,775 87,370 134,338 133,775 87,370 134,338 133,775 87,370 134,338 133,775 87,370 134,338 133,775 87,370 134,338 133,775 87,370 134,338 134,338 135,755 134,338 134,338 135,755 134,338 134,338 135,755 134,338 134,338 135,755 134,338 134,338 134,338 135,755 134,338 134,338 135,755 134,338 134,338 134,338 135,755 134,338 134,358 134,55858 134,558 134,558 134,558 134,5588 134,5588 134,5588	1601.53 22.249 Mass[ps] 434.121 437.673 436.656 438.075 Mass[ps] 225.145 217.446 212.317.885 317.672 318.675 Mass[ps] 317.672 318.075 Mass[ps] 3158.389	8 Meani[ps] 379.195 378.680 379.527 378.470 Mean[ps] 174.711 173.092 172.598 171.894 171.894 173.992 172.598 171.894 Mean[ps] 276.570 278.284 277.281 277.281 277.281 277.281 277.2947 Mean[ps] 95.648	BP5 BP5 StdDev[ps] 47.872 50.574 50.128 50.574 23.660 23.660 23.374 26.477 23.975 StdDev[ps] 27.221 27.843 StdDev[ps] 27.843 StdDev[ps] 27.845 StdDev[ps]	t(wornt)[p2] 57436.92 50560.82 49936.78 51187.86 51187.86 5072.95 51(wornt)[p2] 57436.91 53700.90 49936.78 54319.08 49936.78 54319.08	Ma 255 255 255 355 389 888 422 855 364 200 210 199 200 301 199 200 301 30 30 30 30 30 30 30 30 30 30 30 30 30



Slwave: Decoupling Capacitor Optimization



Power Integrity Investigation



Release v2014.0



Power Integrity Investigation





Release v2014.0



Investigate Available Decoupling Capacitors

Capacitor Library Browser





Automated Process to Optimize Capacitors



• Genetic Algorithm Setup

- Optimized for Impedance
- Optimized for Total Number of Capacitors
- Optimized for Capacitor Types
- Optimized for Price



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PI Advisor: Automated PI Analysis ANSYS°

SV HG

- Optimizes Decoupling Capacitors for Power Integrity
- Time = 15 min 7 sec
 - Frequency Setup
 - 1KHz <= f < 1GH7
- Original solution
 - Total # Caps: 74
- Optimized Solution
 - Total # Caps: 18
 - Capacitor Types = 5
 - AVX, Samsung, and Kemet





Slwave: PCIe 8GT/s Channel Example





PCIe Gen 3 DOE Channel Simulation



Tx:

- •8 GT/s
- •125 ps UI
- •25 ps rise & fall times

Rx:

- •1 tap DFE
- 1st Order CTLE



Symbol	Parameter	Value	Units	Comments
V _{RX-CH-EH}	Eye height	25 (min)	mVPP	Eye height at BER=10 ⁻¹²
T _{RX-CH-EW}	Eye width at zero crossing	0.3 (min)	UI	Eye width at BER=10 ⁻¹²
T _{RX-DS-OFFSET}	Peak EH offset from UI center	+/- 0.1	UI	
V _{RX-DFE_COEFF}	Range for DFE d ₁ coefficient	+/- 30	mV	Feedback coefficient

















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ANSYS User Defined Document (UDD)









- Slwave merged with Alinks to provide a very cohesive flow from import to simulation.
- Slwave has multiple solver technology options for the users needs.
 - Power integrity and signal integrity
- Slwave can be used solely as a front end tool or linked with DesignerSI to handle any type of post validation channel simulation.
- UDO and UDD within Designer enable users to customize and easily create validation kits and report generation.
- The ANSYS post validation solution backed with accurate electromagnetic models allows root cause trouble shooting and optimization.



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Peter Krenz, Application Engineer