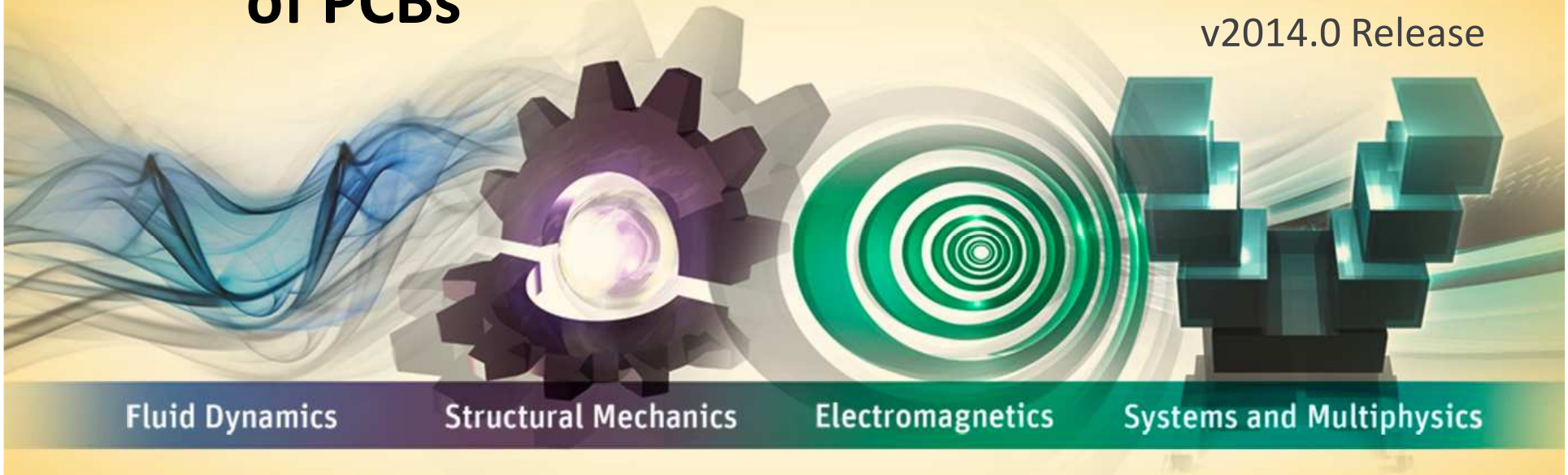
ANSYS

Realize Your Product Promise®

Modern Simulation Solutions for Signal and Power Integrity for Efficient Design of PCBs

v2014.0 Release



Peter Krenz, Application Engineer

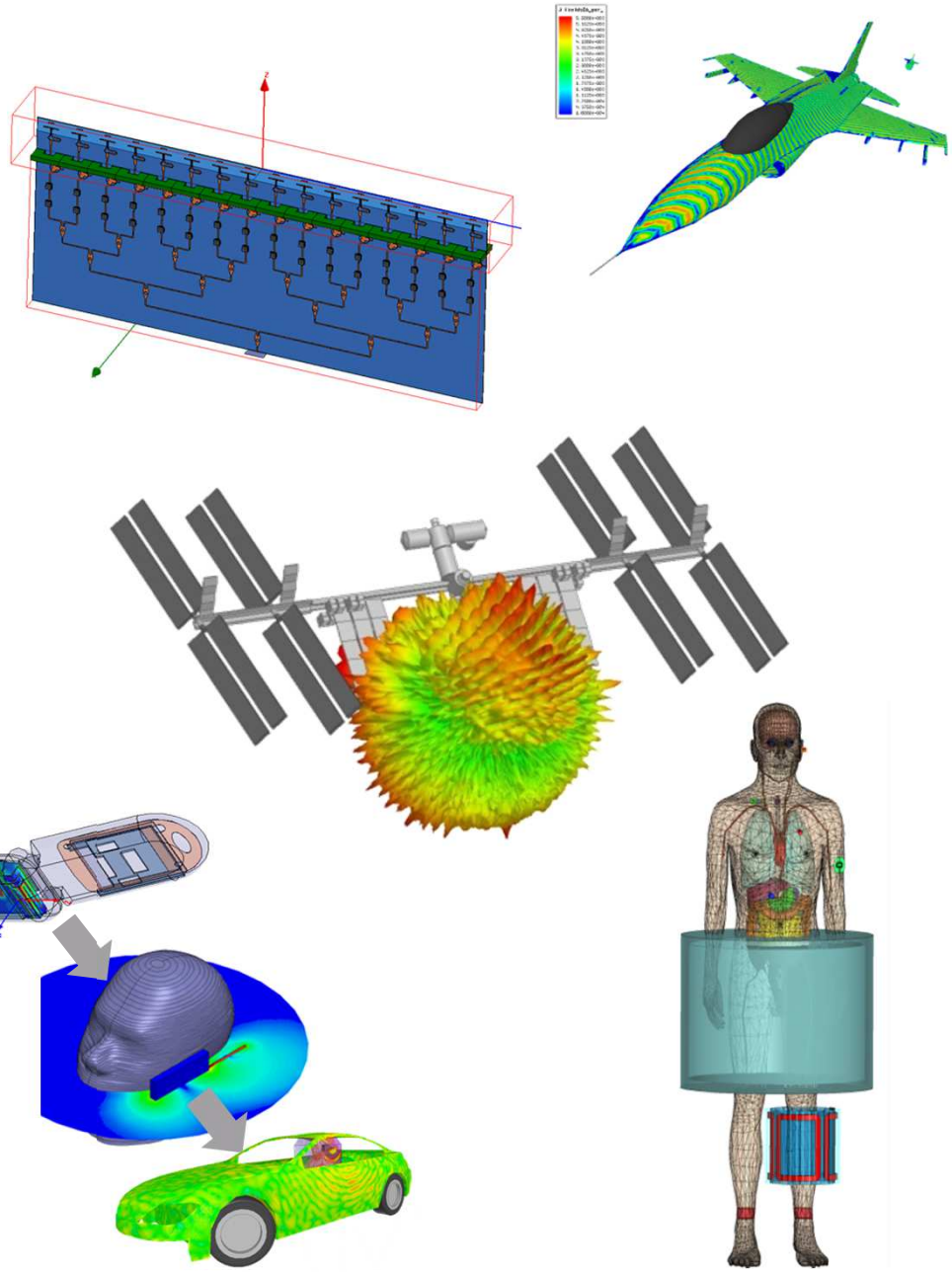
Agenda

- **Introduction**
  - High Frequency Simulation Tools Overview
  - Cannel Simulation Flow
- **SIwave Capabilities**
- **Test case:**
  - Decoupling Capacitor Optimization
  - PCI Express 8 GT/s Channel
- **Summary**

ANSYS:
High Frequency Applications Overview

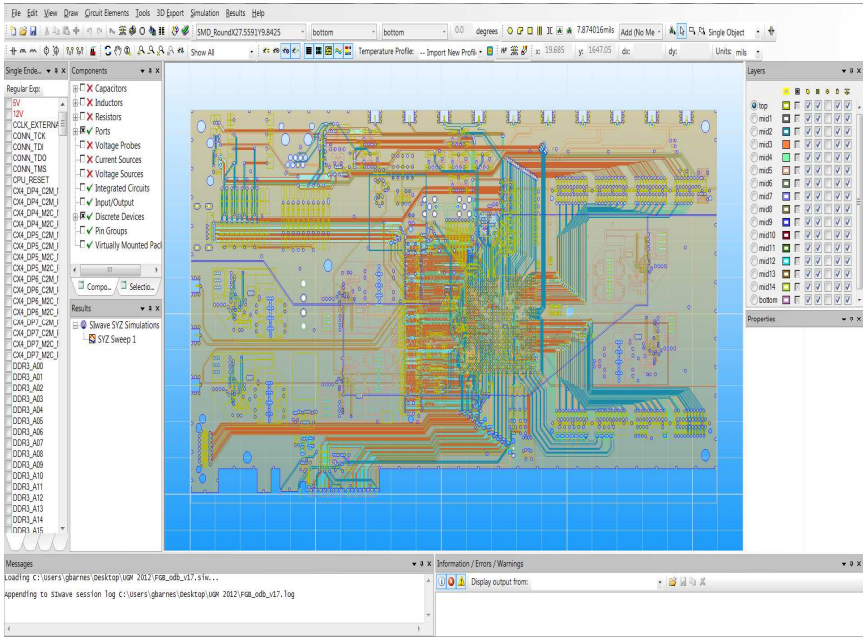
What is HFSS?

- **Premier 3D Electromagnetic design tool**
- **Solves**
  - Any arbitrary 3D structure
- **Uses**
  - Full Wave Finite Element Method (FEM)
  - Transient Finite Element Solver
  - Integral Equation Solver
  - Physical Optics Solver



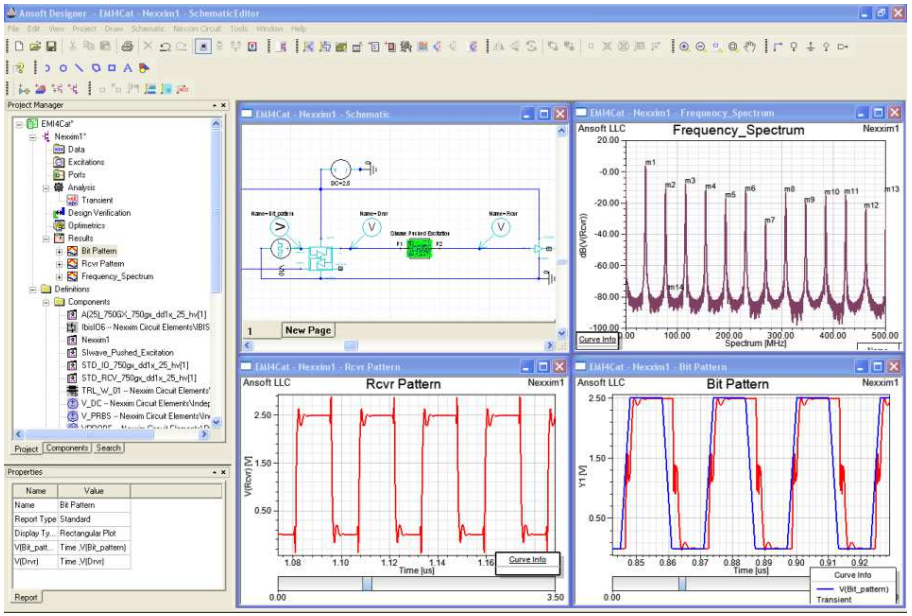
What is SIwave?

- **ANSYS SIwave evaluates designs from entire package, board, or package on board**
- **SIwave includes all effects of coupling between traces, packages, and board**
  - Advanced Signal- and Power-Integrity Analysis
  - Easy Layout Extraction (S,Y,Z)
  - Automated Decoupling Capacitor Optimization
  - Integrated and Automated DC I^2R Reporting
  - Advanced Broadband SPICE Model Generation
  - Highly Accurate Macro Modeling
  - High-Performance Computing
  - Comprehensive Multi-physics (Icepak)



What is Designer?

- **Integrates ANSYS HF tools into a seamless system simulation**
- **Solves**
  - Time / frequency circuits and systems
- **Uses**
  - State Space or convolution time domain spice solver
  - Harmonic Balance frequency domain solver
  - 2D / 3D Method of Moment solver
- **Applications**
  - Time and / or frequency domain circuit analysis
  - Signal Integrity
  - Antenna Arrays
  - RF IC simulation

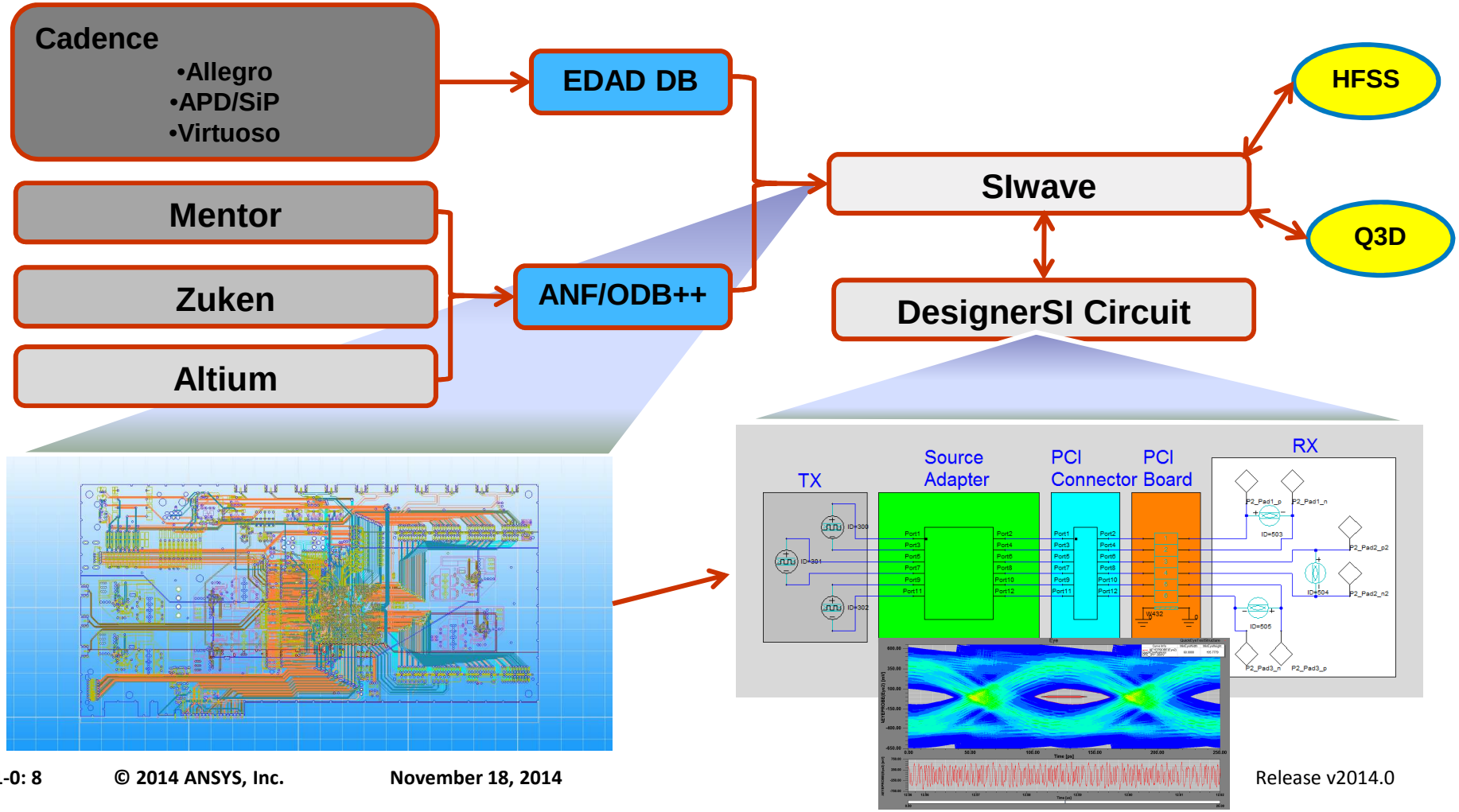


SIwave:
Channel Simulation Flow

Introduction: Channel Simulation Flow

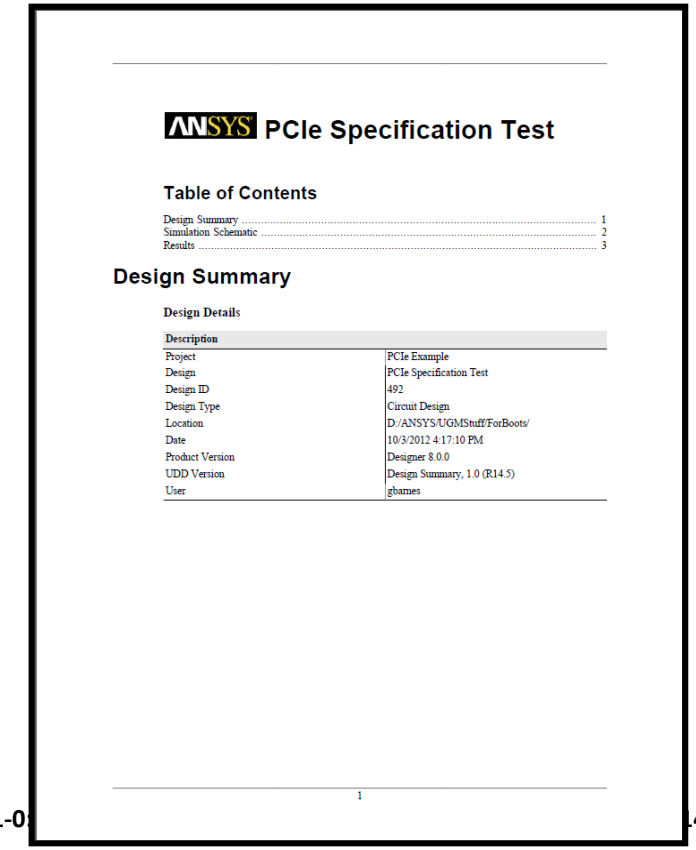
Post layout validation → Simulate the physical architectures, create electromagnetic-based models, and apply time domain signaling in conjunction with these models.

ANSYS has streamlined this process for engineers with the use of one product: *SIwave*



Introduction

- A pass/fail solution quickly shows engineers if their design is sufficient or not.
- ANSYS Solution ⇨ Gold Standard Accuracy with Parasitic Extraction
- Each component of the channel can be decomposed, studied, and optimized
- This solution provides the **Why**



ANSYS PCIe Specification Test

Table of Contents

Design Summary

Design Details

Description	
Project	PCIe Example
Design	PCIe Specification Test
Design ID	492
Design Type	Circuit Design
Location	D:/ANSYS/UGMStuff/ForBoots/
Date	10/3/2012 4:17:10 PM
Product Version	Designer 8.0.0
UDD Version	Design Summary, 1.0 (R14.5)
User	gbarnes

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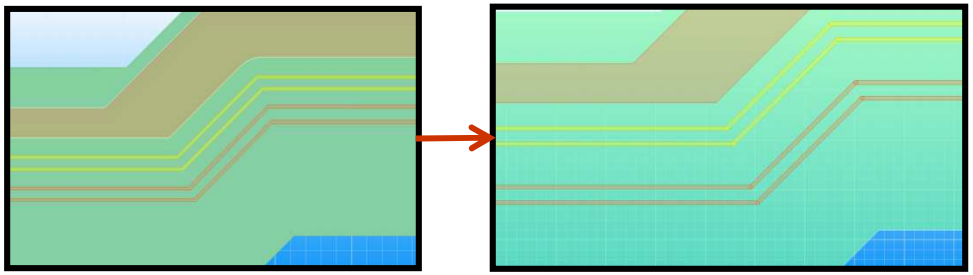

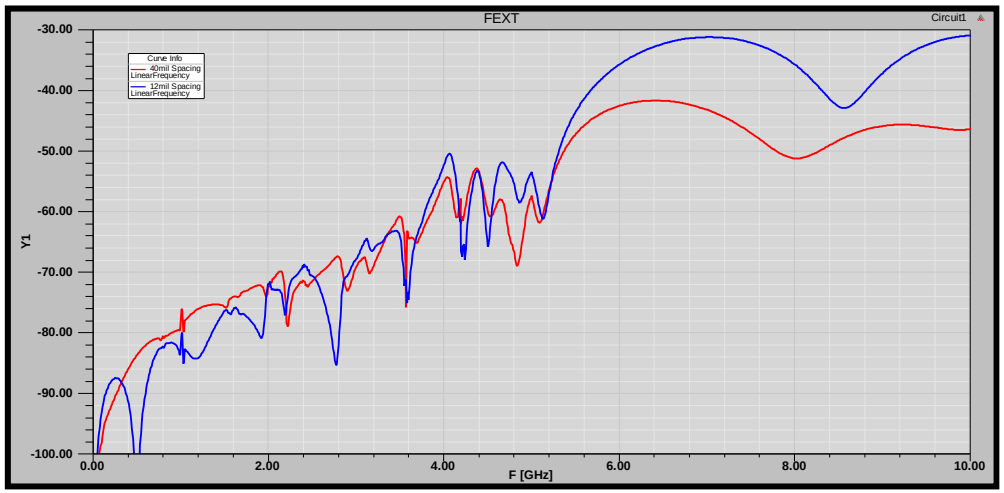

ANSYS

SIwave:
Power and Signal Integrity Extractor

What is SIwave?

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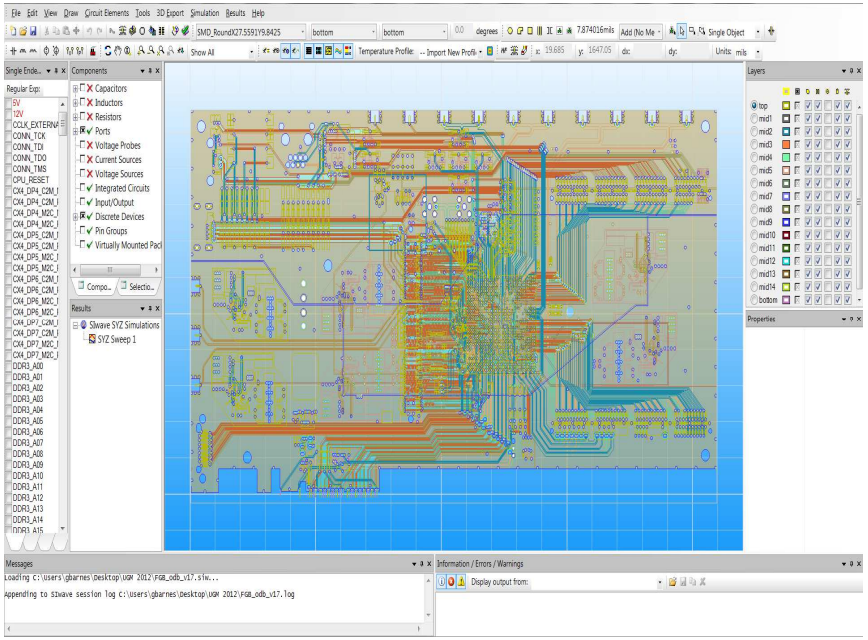
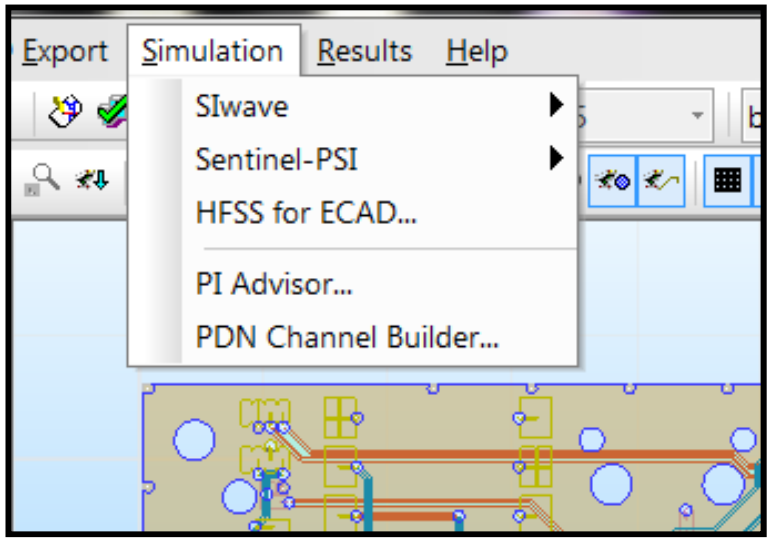
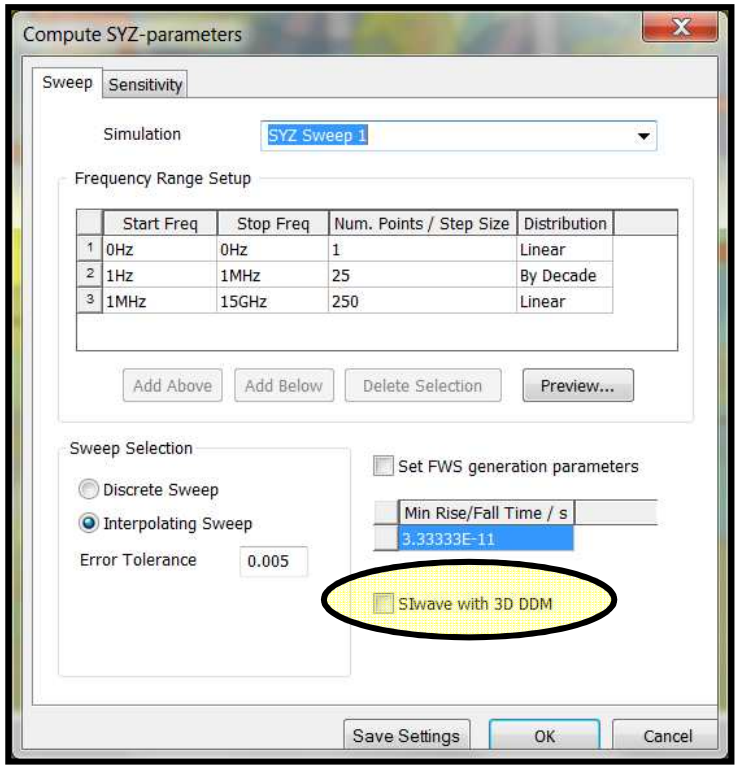


SIwave: More Than 2.5D





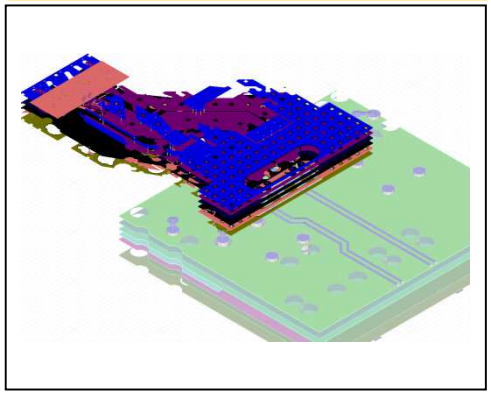
- **SIwave 2.5D Full wave Hybrid solver**
- **SIwave 2.5D Full wave Hybrid solver + Q3d**
- **HFSS 3D Full Wave FEM**

Full-Wave Package/Board Positioning

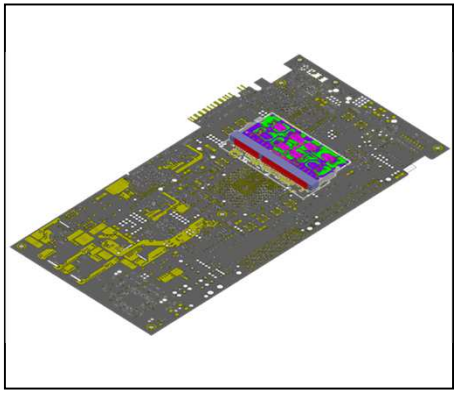
Arbitrary 3D → **Hybrid**

Arbitrary 3D Electromagnetics → **Board + Package** → **SPEED**

HFSS-Solver on Demand



SIwave



SI

- Golden Accuracy Simulator
- Solves Any 3D geometry
- Powerful for Critical Nets
- Layout Front-end for HFSS

Any Geometry

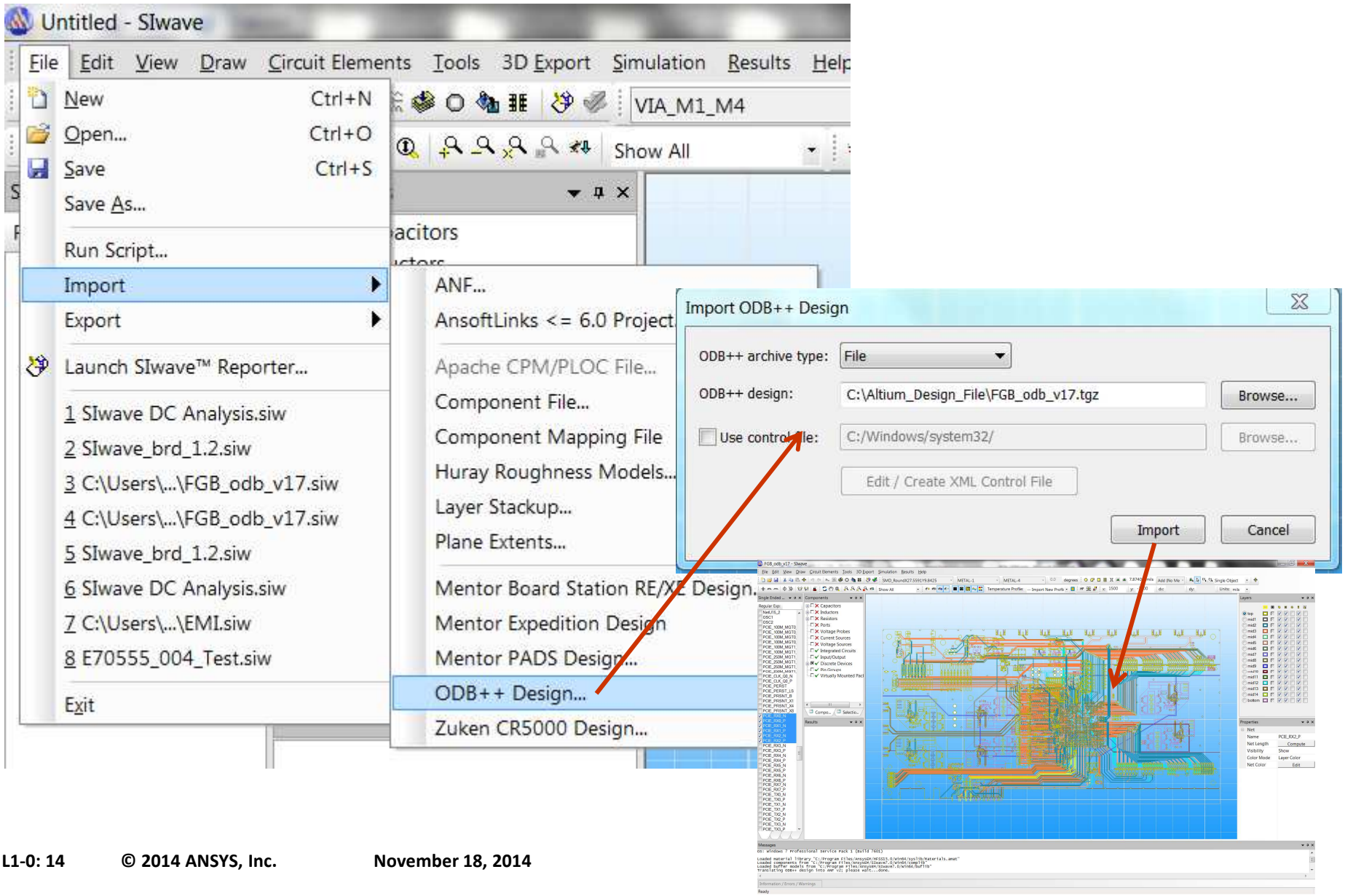
Gold Standard Accuracy

SI/PI

- FAST Hybrid method for PKG/BRD
- Marked ease of interaction with Complicated Board geometries
- Handles many, but not all 3D effects

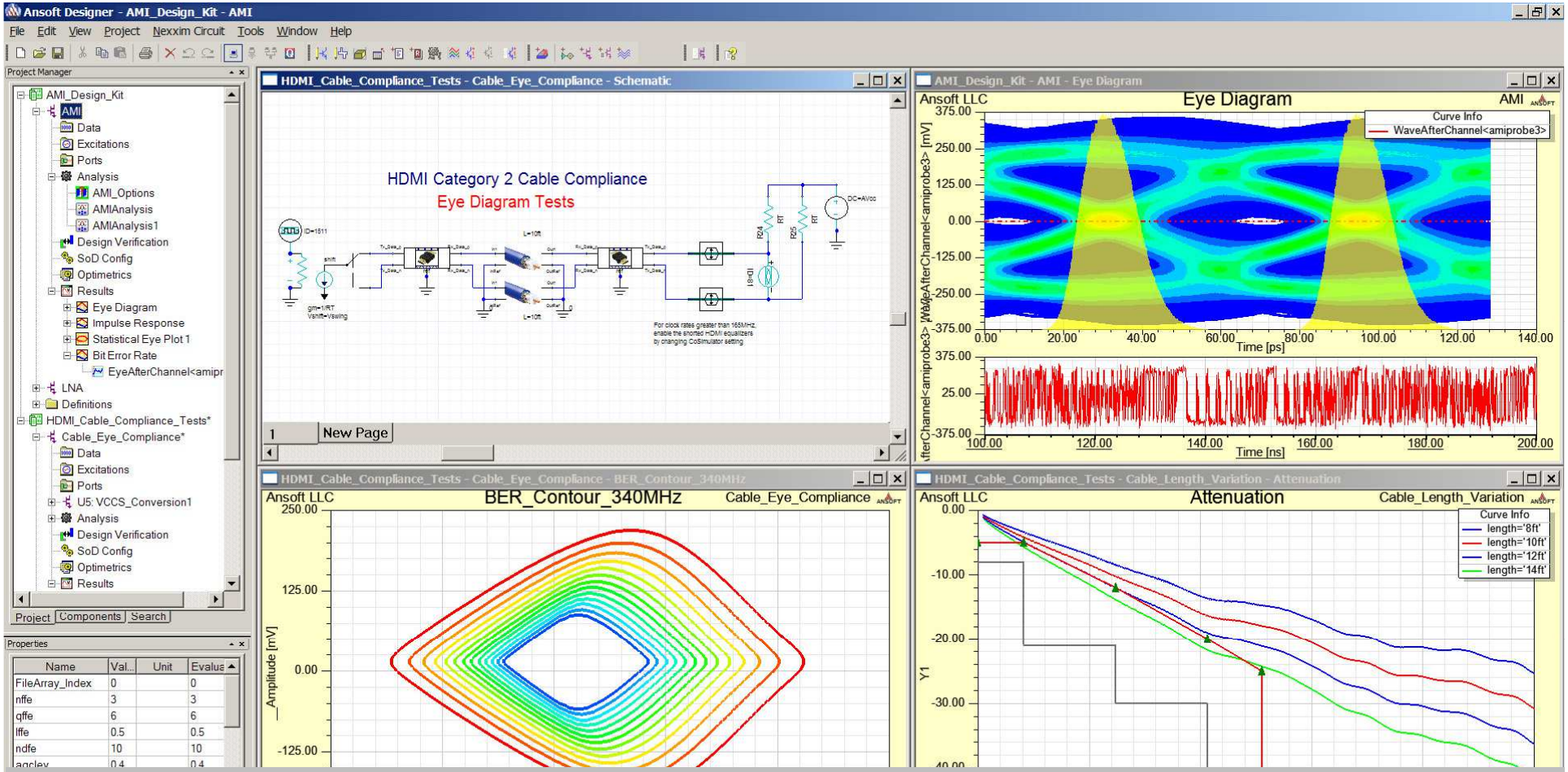
Fast

SIwave Includes Alinks for EDA



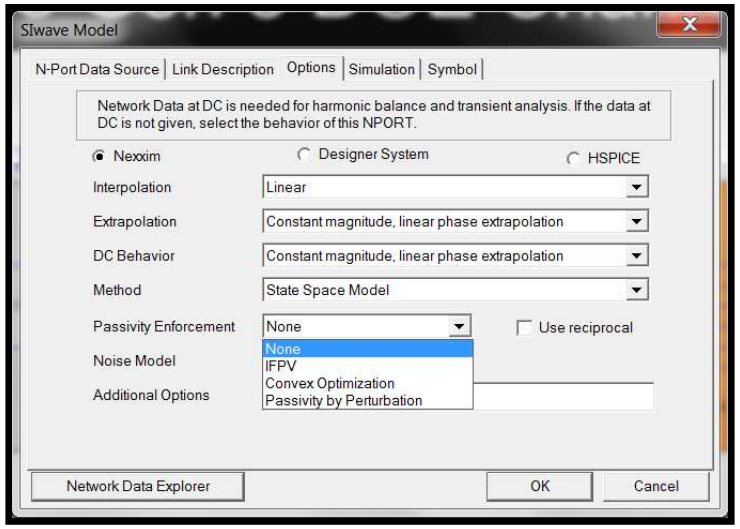
SIwave:
NEW DesignerSI Circuit Capability

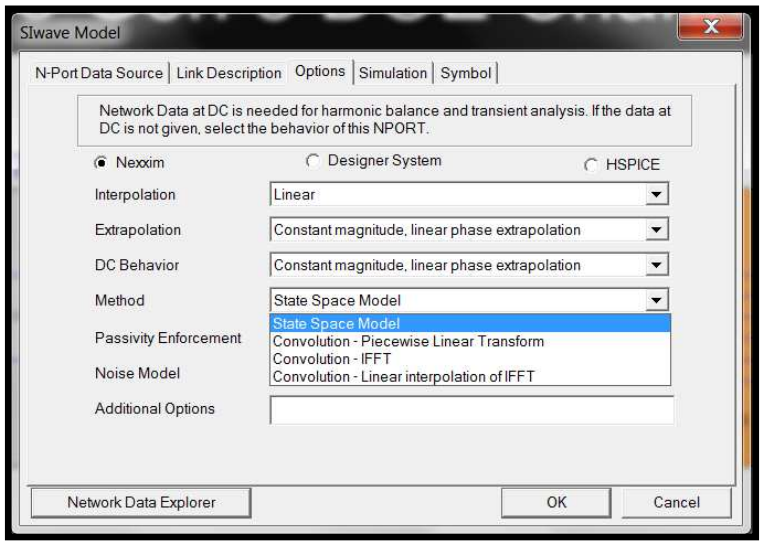
Designer for SI



- Circuit Simulator- Nexxim Engine (transient, fast convolution, statistical and IBIS-AMI circuit simulation)
- Integrated Schematic capture and layout tool
- Design management front-end linking EM simulation products (HFSS, Q3D, SIwave, ..)
- 2D quasi-static field solver
- HFSS Solver on Demand

Nexxim Engine: Simulation Piece of Mind





Models extracted out from our electromagnetic solvers are handled correctly.

Nexxim engine can ensure that the models you run are causal and passive in the time domain.

Nexxim will enforce these criteria for outside models as well.

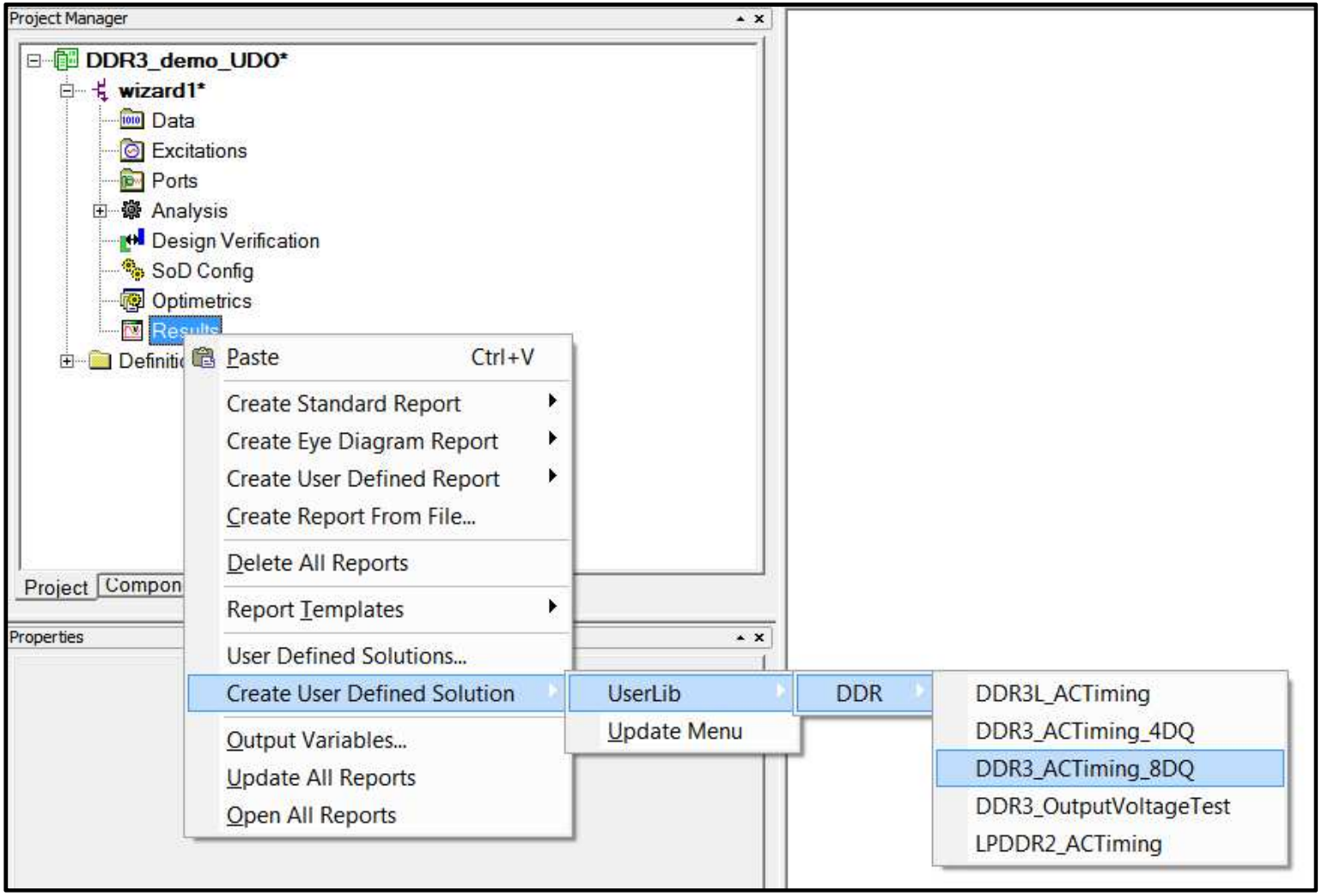
User can just click the option and go. There is no guess work!

What is ANSYS UDO?

- **UDO (User Defined Outputs) allows calculations and post-processing of use raw transient simulation data**
  - Designer SDF file
  - H-Spice TR0 file

- **Key benefits:**
  - Non-Ideal voltage supply is supported
  - Every bit-by-bit falling and rising transition edge is calculated
  - Fully customizable through Python scripts.
    - UDOs specific to LPDDR, DDR2 and DDR3 standards already exist!

What is an ANSYS UDO?



What is an ANSYS UDD?

- **Example of a potential report created in PDF and HTML format**

ANSYS DDR3
Virtual Compliance Test

Table of Contents

Summary

Overall Results for DDR3 Compliance Test

- **AC Data Timing: 4/5 metrics passed**

Table 1. Configuration Details

System Description	
Speed Grade	DDR3-1600
Voltage Level	AC150
Spec Version	JESD79-3E
Test Summary	
Project	Non-IP_DDR3_Example
Design	DDR3_W_elements_dynamic_link
Variation	$CPU_Corner_Index="typ" $CPU_RX_ODT_Strength_Index="DIN_ODT_OFF" $Dimm_BRD_Index="$PROJECTDIR\DIMM_BRD\DIMM_Models\SSS\DIMM_Module_Byte_0_20.sss" $Dimm_Corner_Index="typ" $IO_DRV_Strength_Index="DQ_DRV_34" $Main_BRD_Index="$PROJECTDIR\Main_BRD\Models\SSS\Main_BRD_Byte_1_20.sss" $UI=6.25e-010s' CPU_PKG_L='0.5in' Dimm_PKG_L='0.5in'
Location	C:\Ansoft\Projects_VirtualCompliance\Steve_IP_FREE_Example
Date	12/22/2011 8:47:14 AM
Product Version	7.0
UDD Version	1.08
User	bboots

AC Data Timing

Verification of Electrical Characteristics and AC Timing for Data (JESD79-3E)

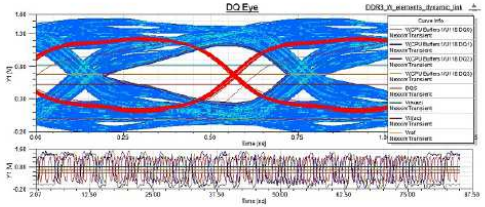
1

ANSYS DDR3 Virtual Compliance Test

Measurement Results

Table 2. Data Timing Results - All DQ, All Edges (Sec 13.1)

Metric	Worst Actual	Worst Margin	Spec Value	Unit	Notes
tDS(base)	252.256	242.256	10	ps	
tDH(base)	87.370	42.370	45	ps	
tDS(derated)	208.386	198.386	10	ps	
tDH(derated)	9.370	-35.629	45	ps	
tDQSQ	94.661	5.338	100	ps	t(worst)=56807.334ps



Setup

Table 3. User Defined Solution Configuration

Description	
Solution Name	DDR3 AC-Timing 4-DQ1
Description	Compute DDR3 AC Timing Margines for 4-DQ
UDO Version	1.08
Probes	
VDD	Vdd
DQS	V(CPU Buffers1/U118.DQS_P)
DQS#	V(CPU Buffers1/U118.DQS_N)
DQ0	V(CPU Buffers1/U118.DQ0)
DQ1	V(CPU Buffers1/U118.DQ1)
DQ2	V(CPU Buffers1/U118.DQ2)
DQ3	V(CPU Buffers1/U118.DQ3)
Properties	
AC DQ Level	AC150
Speed Bin	Auto (from DQS)
DQS delay	447 ps

2

ANSYS DDR3 Virtual Compliance Test

AC and DC Input Levels

Table 4. AC and DC Input Levels

AC and DC Input Levels for Single-Ended Data Signals [V] (Sec 8.1.2)	
Vref	0.675
VIH(dc)	0.775
VIL(dc)	0.575
VIH(ac)	0.825
VIL(ac)	0.525
Differential AC and DC Input Levels [V] (Sec 8.3)	
VIHdiff(ac) Min	0.3
VILdiff(ac) Max	-0.3

Strobe Analysis

Table 5. DQS/DQS# Results

Metric	Value	Unit
Speed Bin	1600	
Mean Frequency	1601.538	BPS
Std Deviation	22.249	BPS

Per DQ Metrics

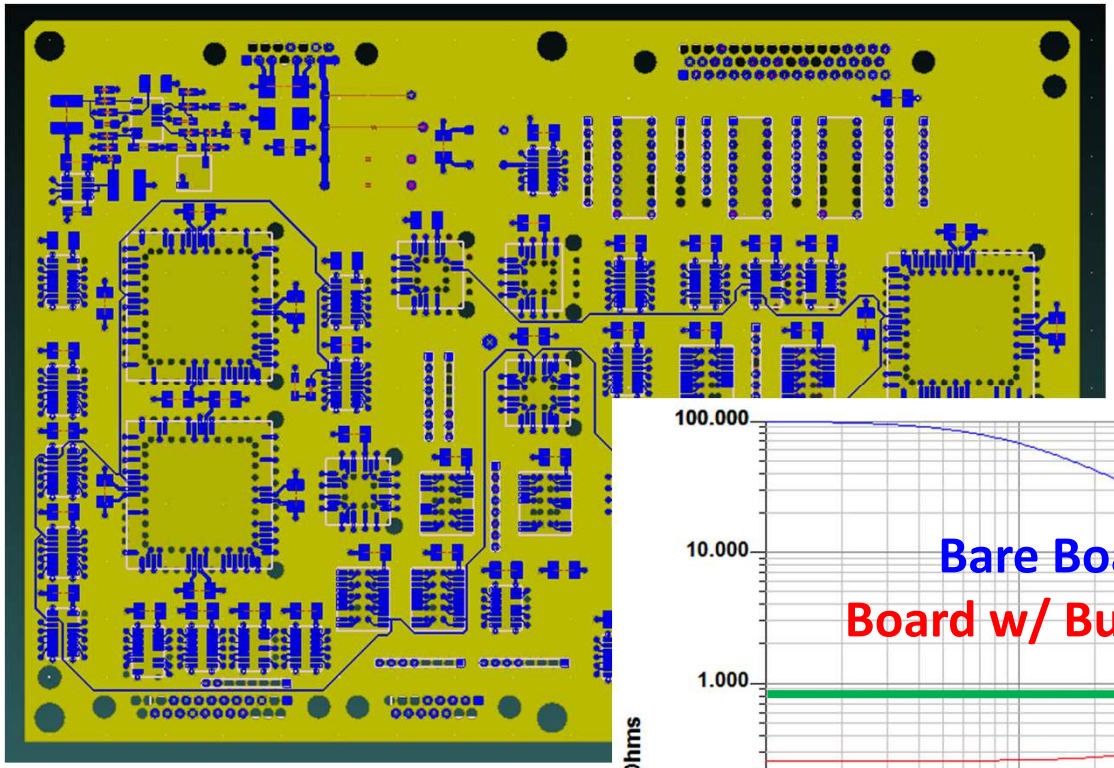
Table 6. Data Line Metrics

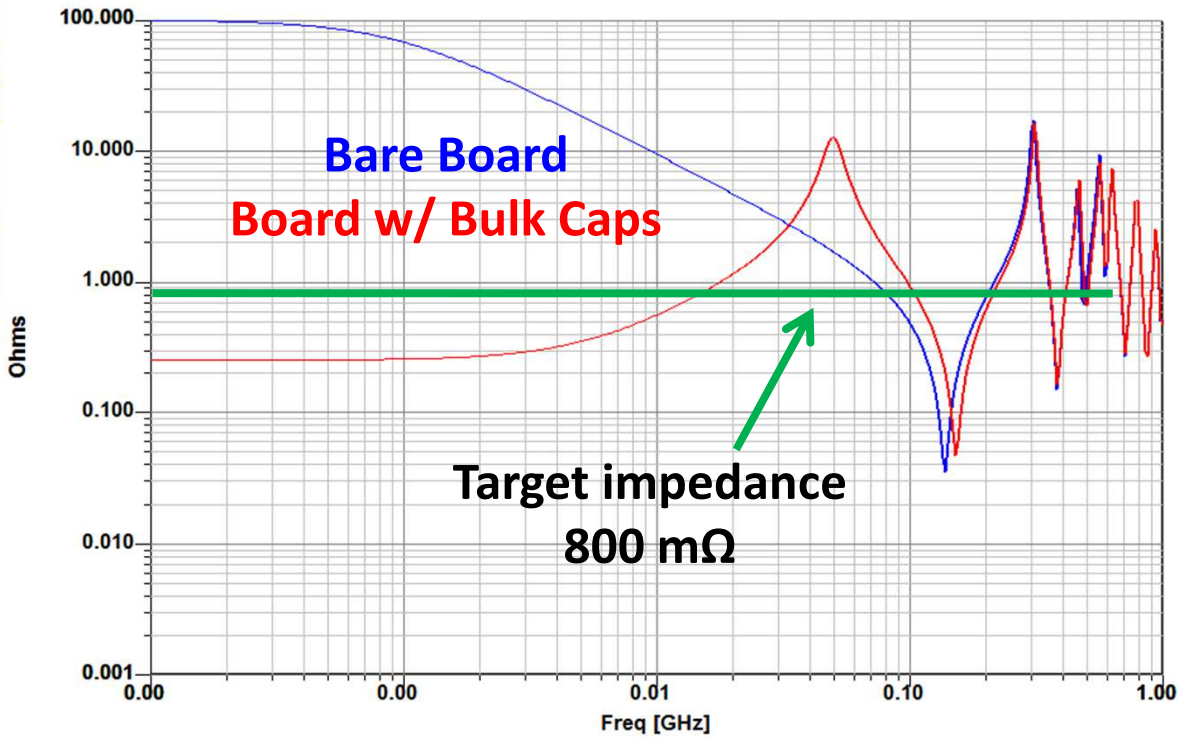
tDS(base)	Min[ps]	Max[ps]	Mean[ps]	StdDev[ps]	t(worst)[ps]	Margin[ps]
0	263.883	434.121	379.195	47.872	57436.92	253.882
1	252.256	437.673	378.690	50.574	50560.82	242.256
2	261.386	436.566	379.527	50.128	49936.78	251.386
3	262.872	438.075	378.470	49.825	51187.86	252.872
tDH(base)	**Min[ps]**	**Max[ps]**	**Mean[ps]**	**StdDev[ps]**	**t(worst)[ps]**	**Margin[ps]**
0	134.338	228.389	174.711	23.660	27440.77	89.338
1	133.775	225.145	173.092	25.374	76189.79	88.775
2	87.370	217.446	172.598	26.477	2505.29	42.370
3	130.352	212.312	171.894	23.975	68072.95	85.352
tDS(derated)	**Min[ps]**	**Max[ps]**	**Mean[ps]**	**StdDev[ps]**	**t(worst)[ps]**	**Margin[ps]**
0	211.882	317.885	276.570	27.221	57436.91	201.882
1	220.399	316.673	278.284	27.843	53700.90	210.399
2	208.386	317.672	277.281	28.468	49936.78	198.386
3	215.646	318.075	277.947	27.316	54319.08	205.646
tDH(derated)	**Min[ps]**	**Max[ps]**	**Mean[ps]**	**StdDev[ps]**	**t(worst)[ps]**	**Margin[ps]**
0	55.338	158.389	95.648	25.449	27440.77	10.338
1	52.775	155.145	94.264	27.368	76189.79	7.775

3

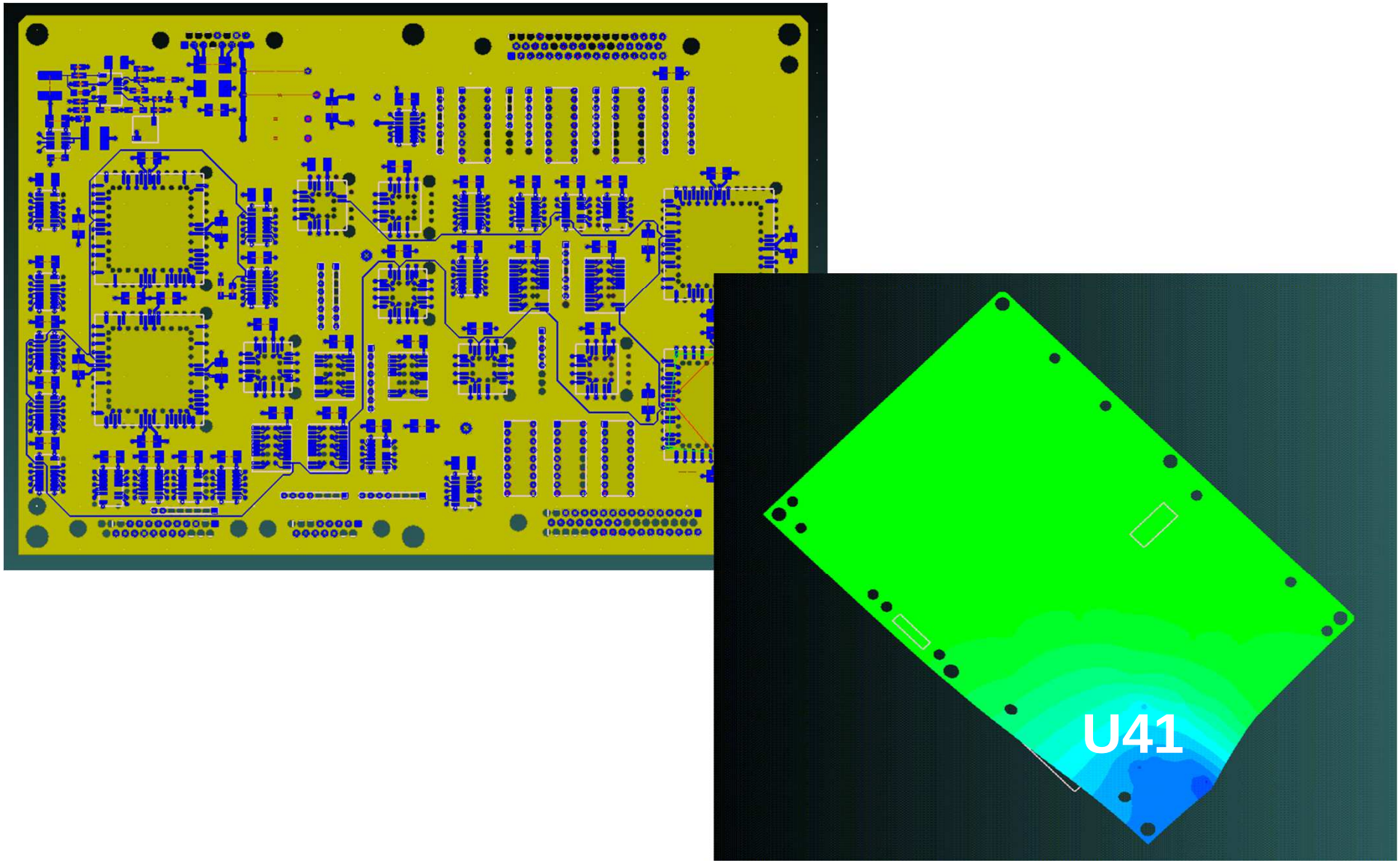
SIwave:
Decoupling Capacitor Optimization

Power Integrity Investigation

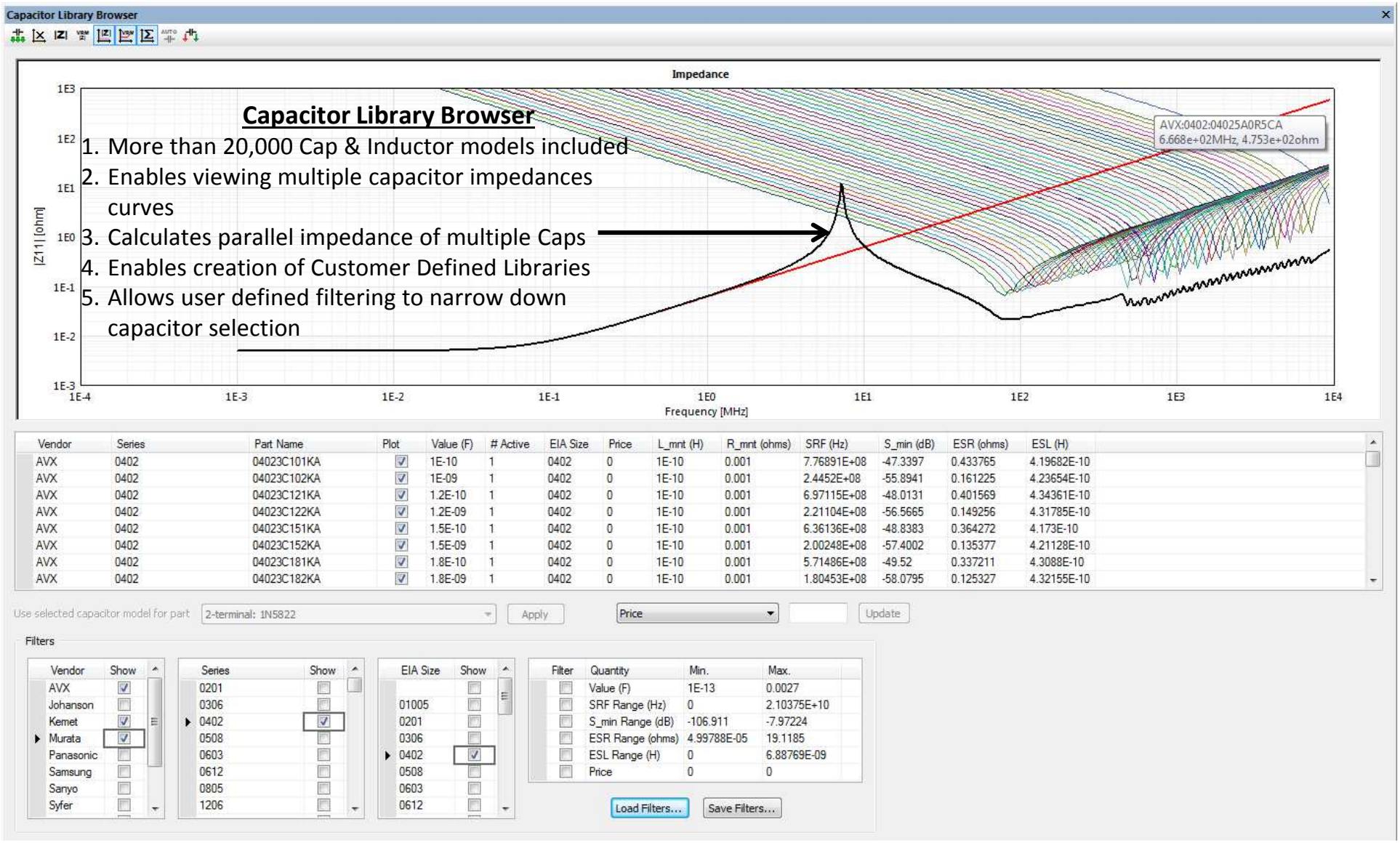




Power Integrity Investigation



Investigate Available Decoupling Capacitors



Vendor	Series	Part Name	Plot	Value (F)	# Active	EIA Size	Price	L_mnt (H)	R_mnt (ohms)	SRF (Hz)	S_min (dB)	ESR (ohms)	ESL (H)
AVX	0402	04023C101KA	☑	1E-10	1	0402	0	1E-10	0.001	7.76891E+08	-47.3397	0.433765	4.19682E-10
AVX	0402	04023C102KA	☑	1E-09	1	0402	0	1E-10	0.001	2.4452E+08	-55.8941	0.161225	4.23654E-10
AVX	0402	04023C121KA	☑	1.2E-10	1	0402	0	1E-10	0.001	6.97115E+08	-48.0131	0.401569	4.34361E-10
AVX	0402	04023C122KA	☑	1.2E-09	1	0402	0	1E-10	0.001	2.21104E+08	-56.5665	0.149256	4.31785E-10
AVX	0402	04023C151KA	☑	1.5E-10	1	0402	0	1E-10	0.001	6.36136E+08	-48.8383	0.364272	4.173E-10
AVX	0402	04023C152KA	☑	1.5E-09	1	0402	0	1E-10	0.001	2.00248E+08	-57.4002	0.135377	4.21128E-10
AVX	0402	04023C181KA	☑	1.8E-10	1	0402	0	1E-10	0.001	5.71486E+08	-49.52	0.337211	4.3088E-10
AVX	0402	04023C182KA	☑	1.8E-09	1	0402	0	1E-10	0.001	1.80453E+08	-58.0795	0.125327	4.32155E-10

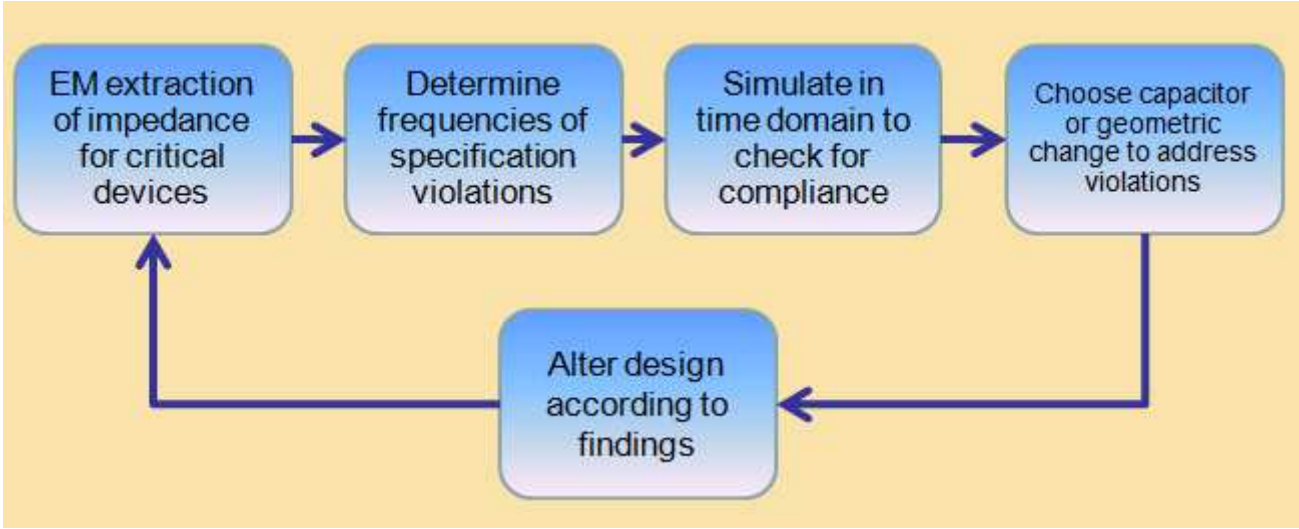
Vendor	Show
AVX	☑
Johanson	☐
Kemet	☑
Murata	☑
Panasonic	☐
Samsung	☐
Sanyo	☐
Syfer	☐

Series	Show
0201	☐
0306	☐
0402	☑
0508	☐
0603	☐
0612	☐
0805	☐
1206	☐

EIA Size	Show
	☐
01005	☐
0201	☐
0306	☐
0402	☑
0508	☐
0603	☐
0612	☐

Filter	Quantity	Min.	Max.
☐	Value (F)	1E-13	0.0027
☐	SRF Range (Hz)	0	2.10375E+10
☐	S_min Range (dB)	-106.911	-7.97224
☐	ESR Range (ohms)	4.99788E-05	19.1185
☐	ESL Range (H)	0	6.88769E-09
☐	Price	0	0

Automated Process to Optimize Capacitors



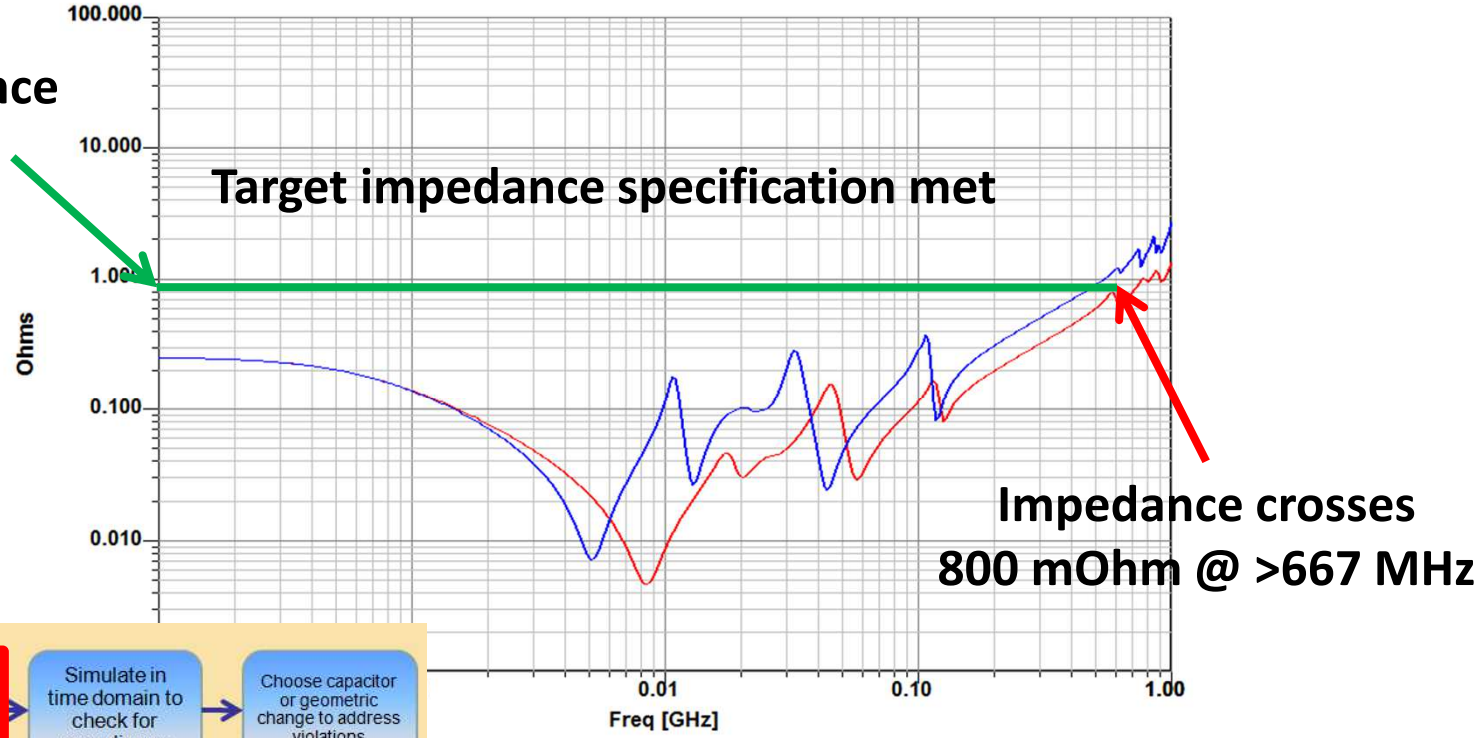
- **Genetic Algorithm Setup**
  - Optimized for Impedance
  - Optimized for Total Number of Capacitors
  - Optimized for Capacitor Types
  - Optimized for Price

Iteration 5: Selecting Capacitors for PI

Board after Iteration 4

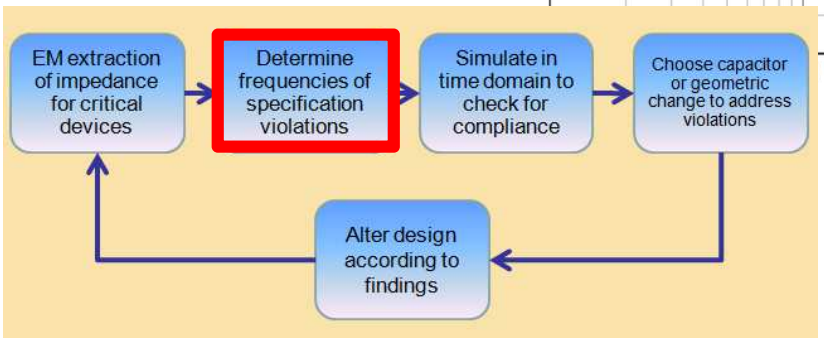
Board after Iteration 5

Target impedance
800 mΩ

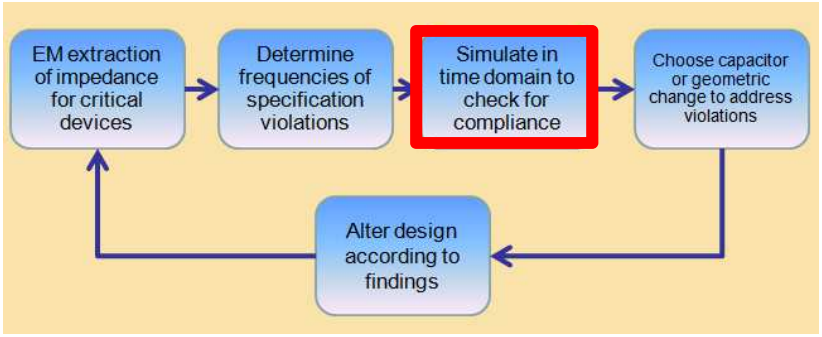


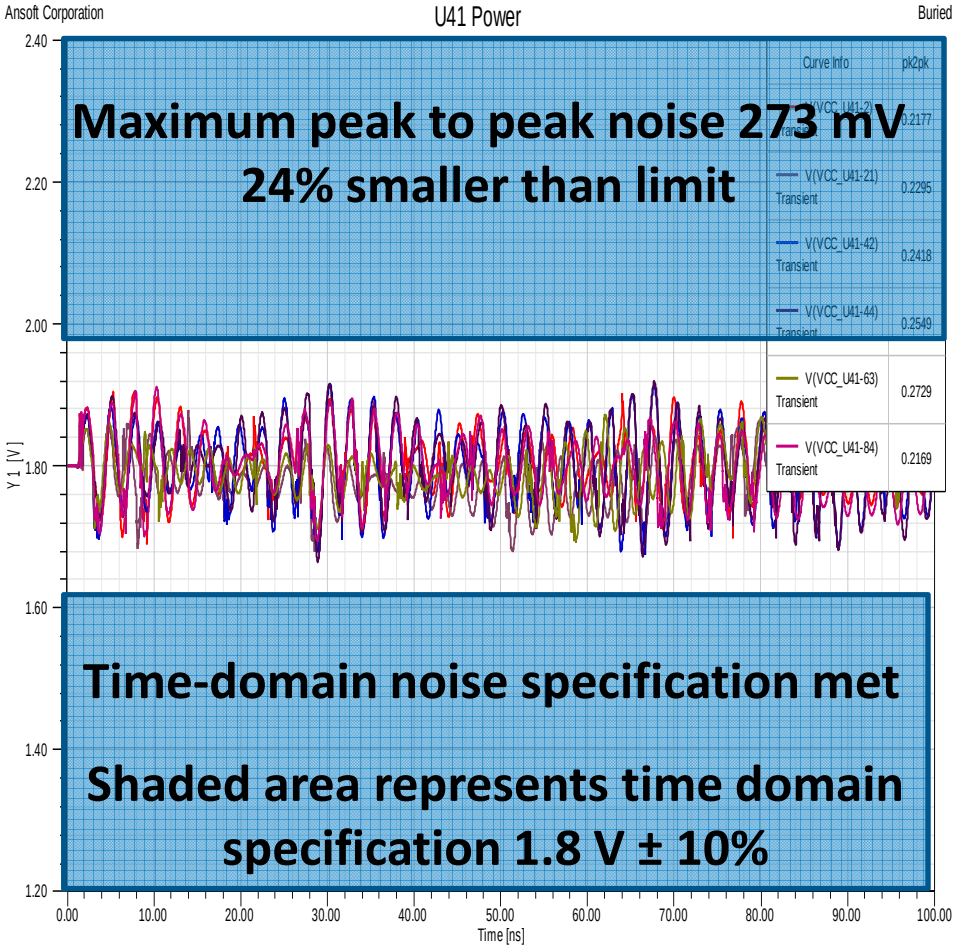
Target impedance specification met

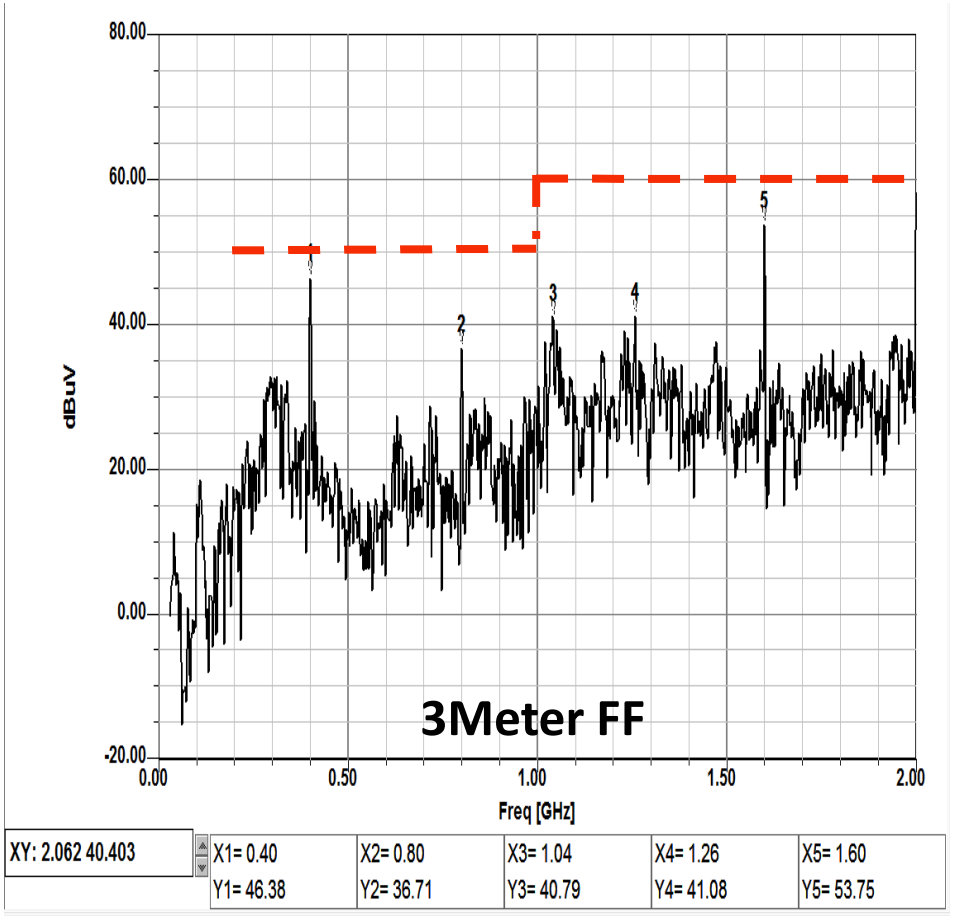
Impedance crosses
800 mOhm @ >667 MHz



Iteration 5

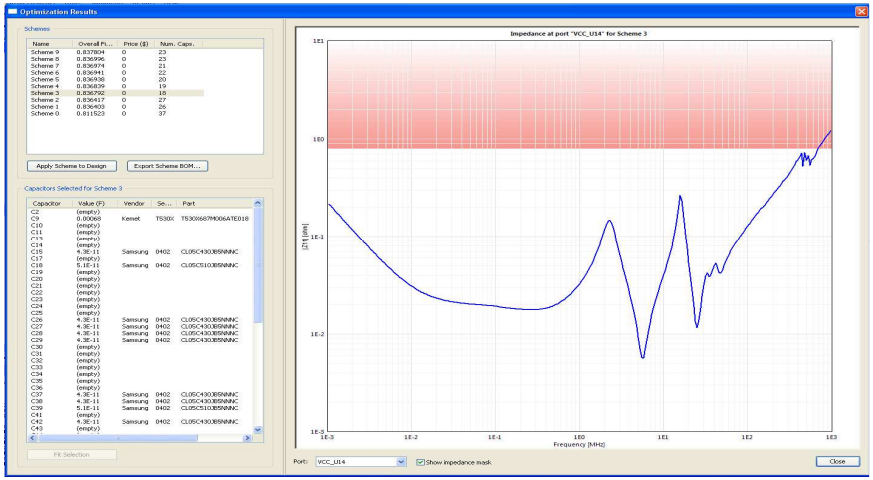


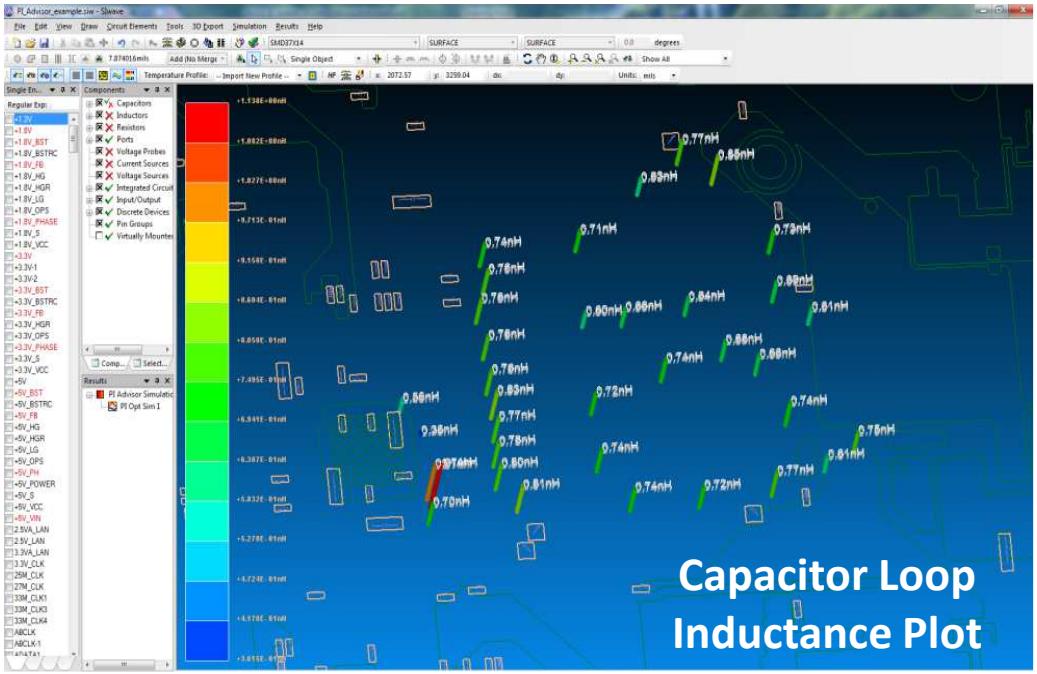




PI Advisor: Automated PI Analysis

- **Optimizes Decoupling Capacitors for Power Integrity**
- **Time = 15 min 7 sec**
  - Frequency Setup
    - 1KHz <= f < 1GHz
- **Original solution**
  - Total # Caps: 74
- **Optimized Solution**
  - **Total # Caps: 18**
  - Capacitor Types = 5
    - AVX, Samsung, and Kemet

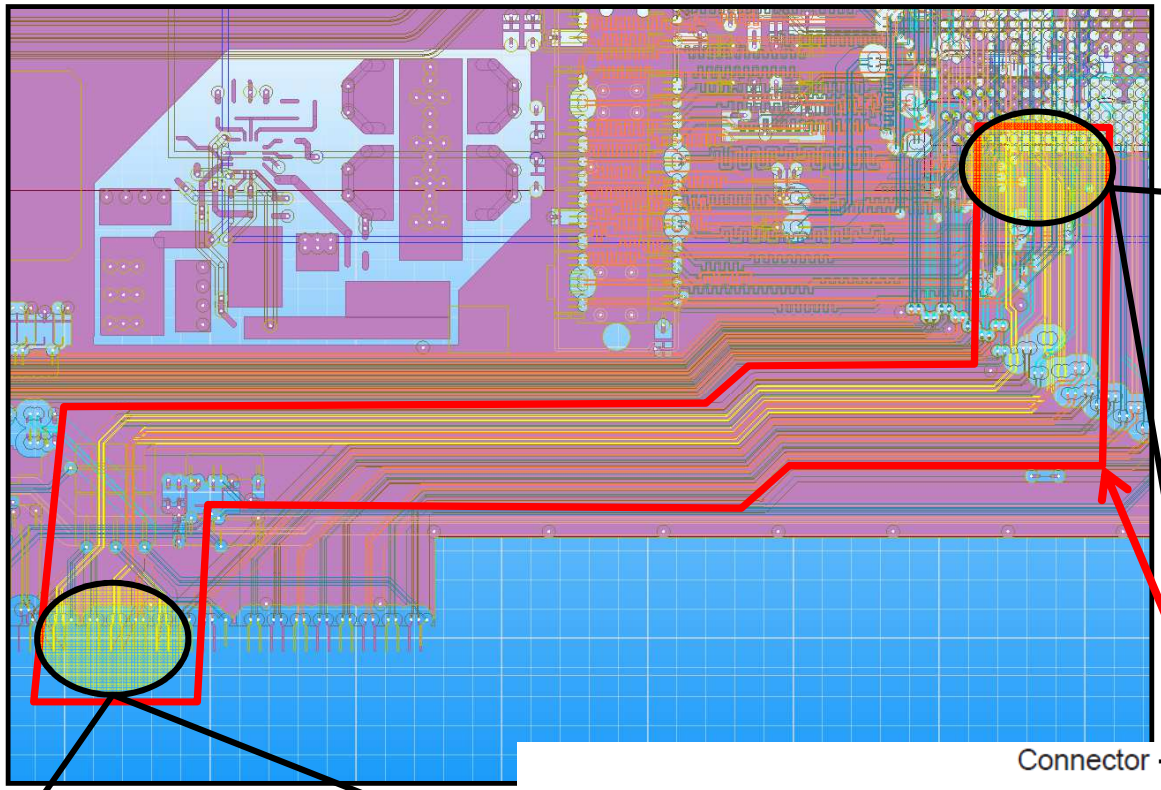


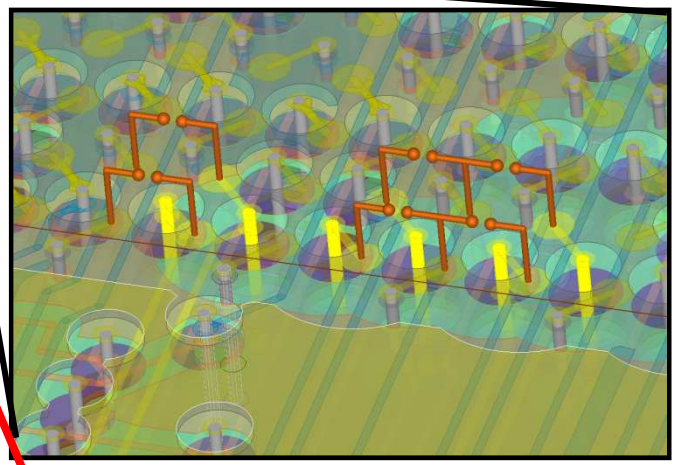


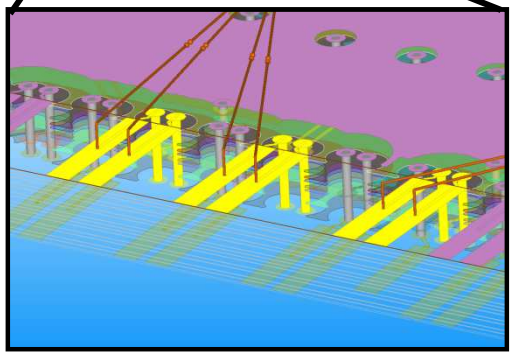
SIwave:
PCIe 8GT/s Channel Example

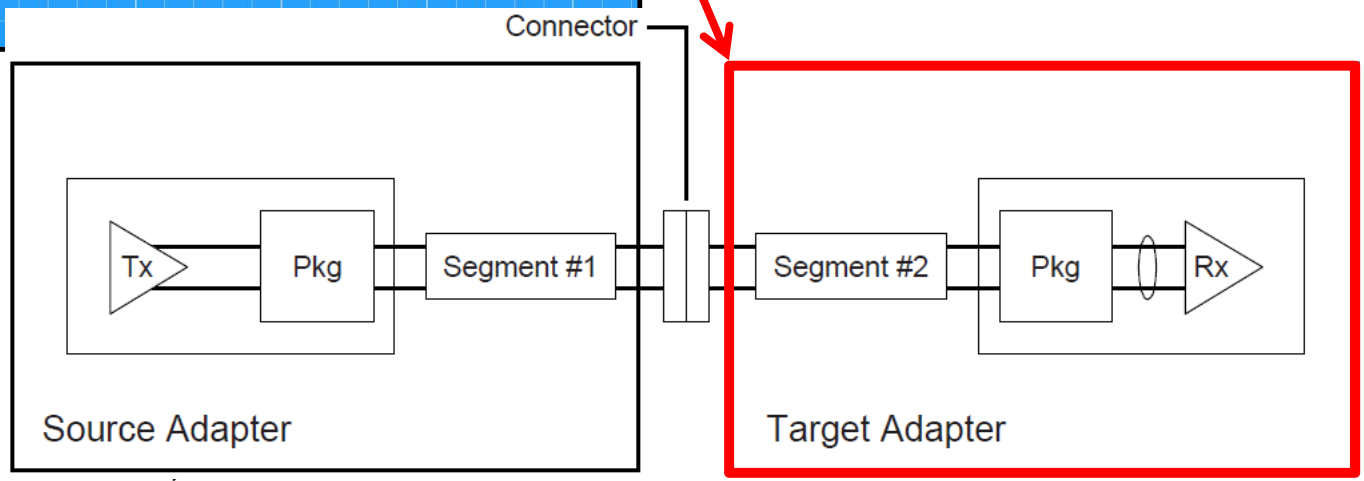
SIwave - PCI Express 8 GT/s channel test case

Three diff pairs on the target Adapter for the edge connector to pads.



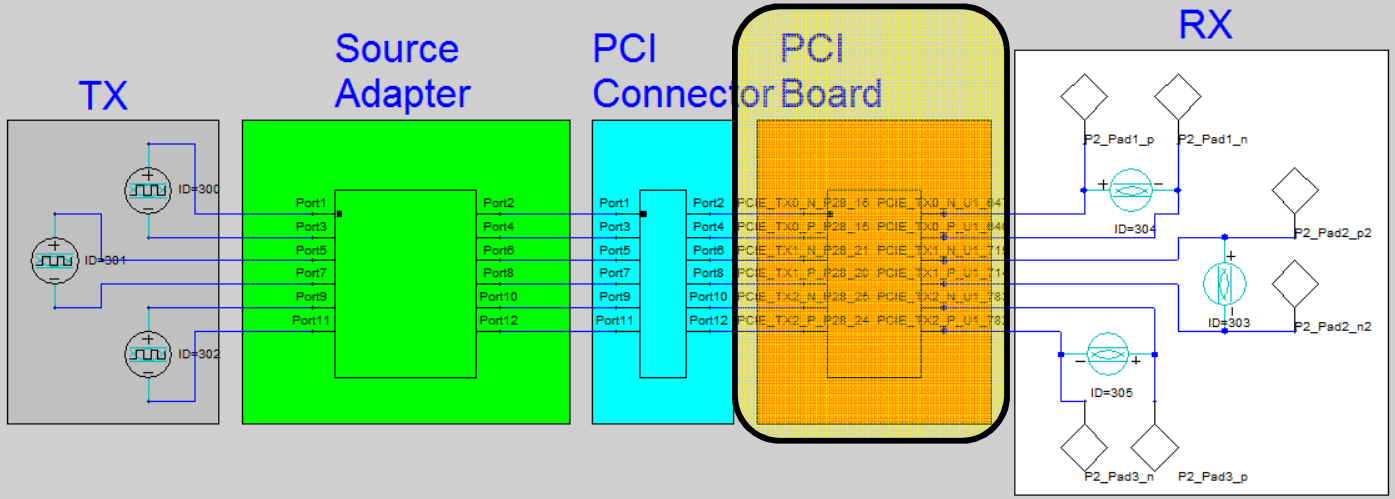






DesignerSI – Time Domain Specification

PCIe Gen 3 DOE Channel Simulation



Tx:

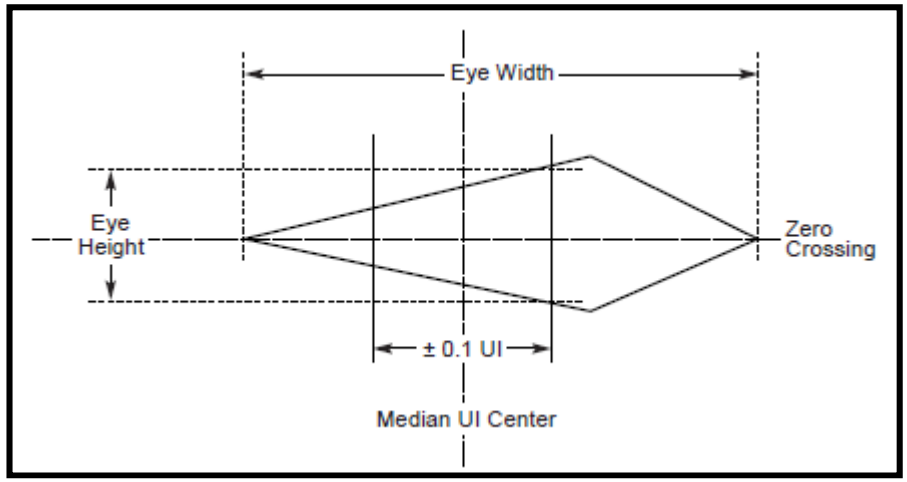
- 8 GT/s
- 125 ps UI
- 25 ps rise & fall times

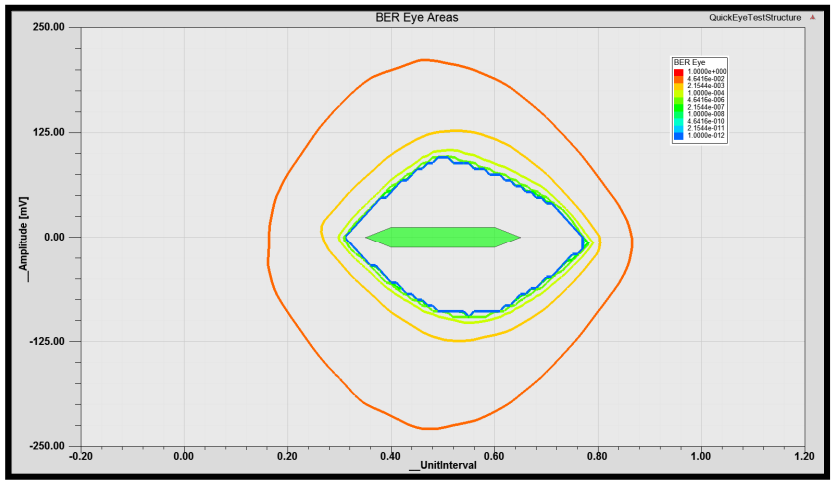
Rx:

- 1 tap DFE
- 1st Order CTLE

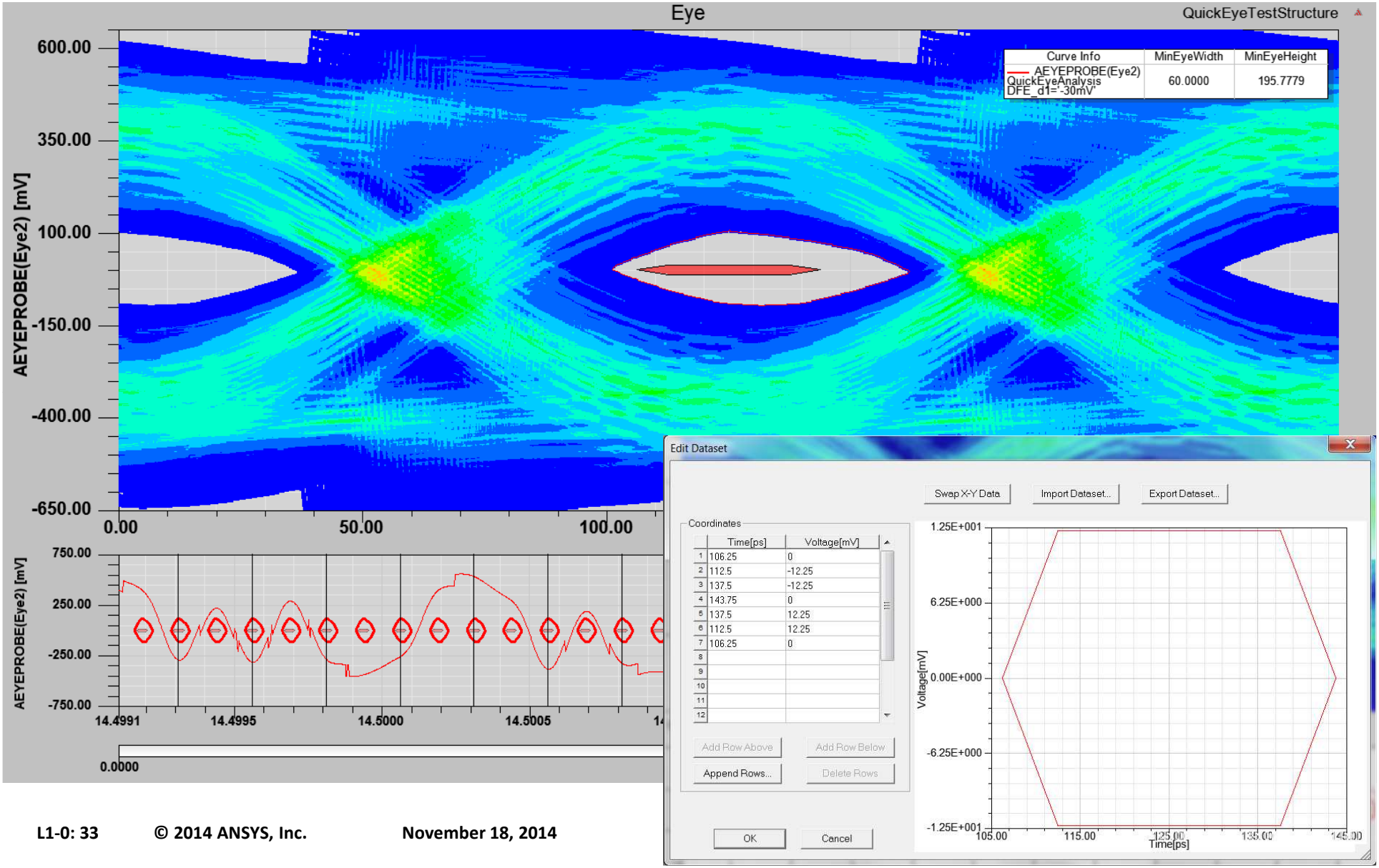
DesignerSI – Time Domain Specification

Symbol	Parameter	Value	Units	Comments
$V_{RX-CH-EH}$	Eye height	25 (min)	mVPP	Eye height at BER=10^{-12}
$T_{RX-CH-EW}$	Eye width at zero crossing	0.3 (min)	UI	Eye width at BER=10^{-12}
$T_{RX-DS-OFFSET}$	Peak EH offset from UI center	+/- 0.1	UI	
V_{RX-DFE_COEFF}	Range for DFE d_1 coefficient	+/- 30	mV	Feedback coefficient

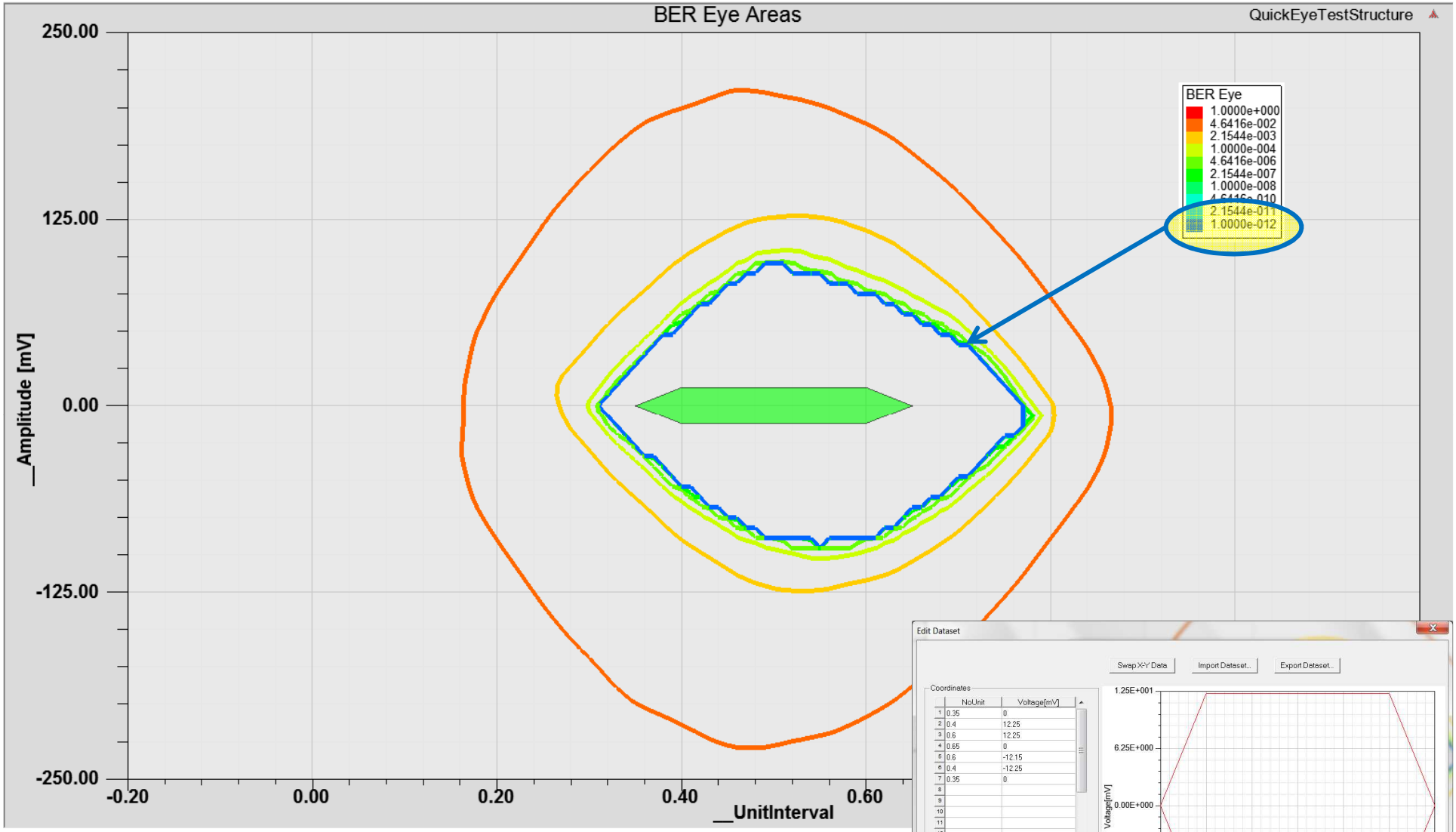




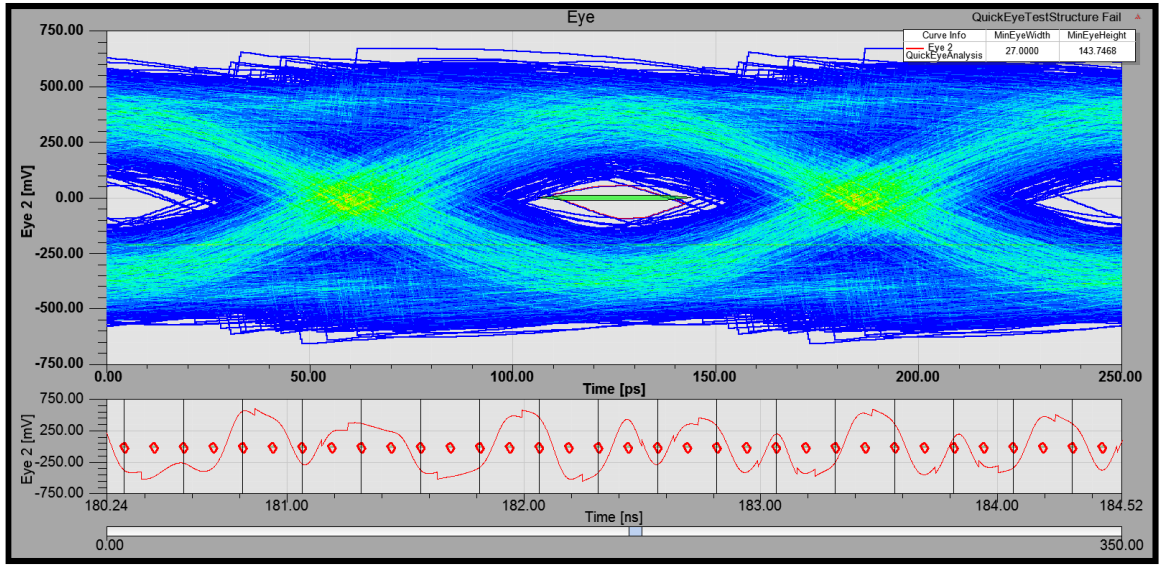
DesignerSI – Time Domain Specification

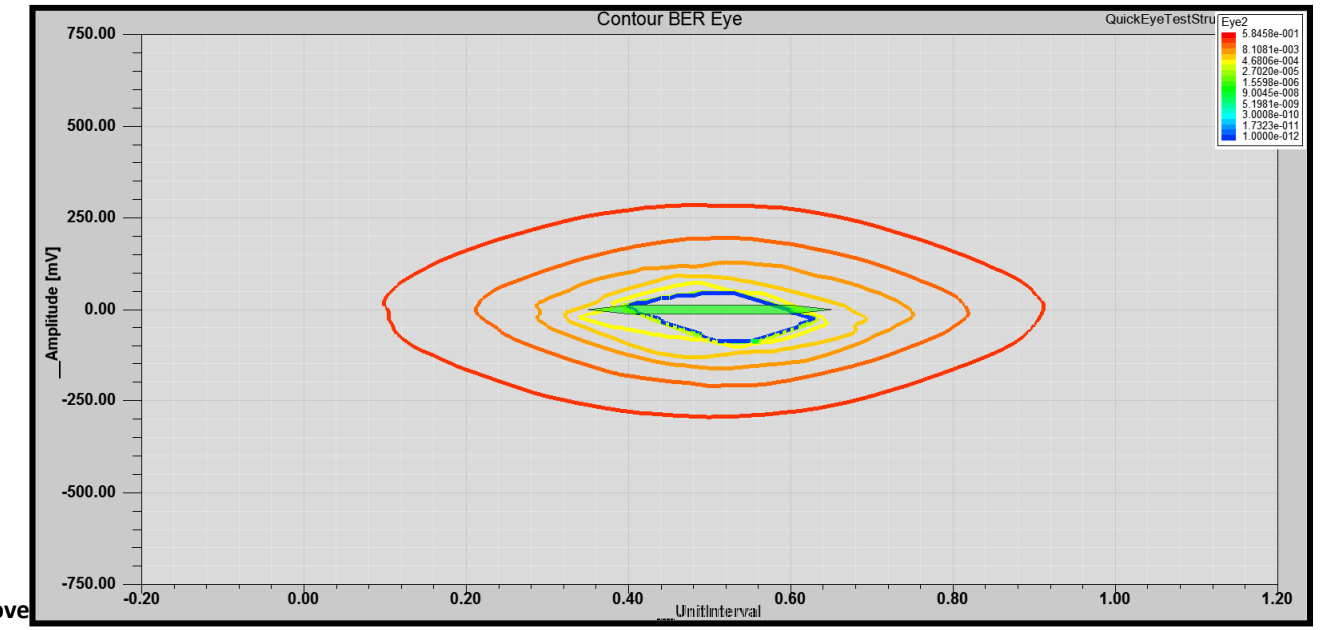


DesignerSI – Time Domain Specification

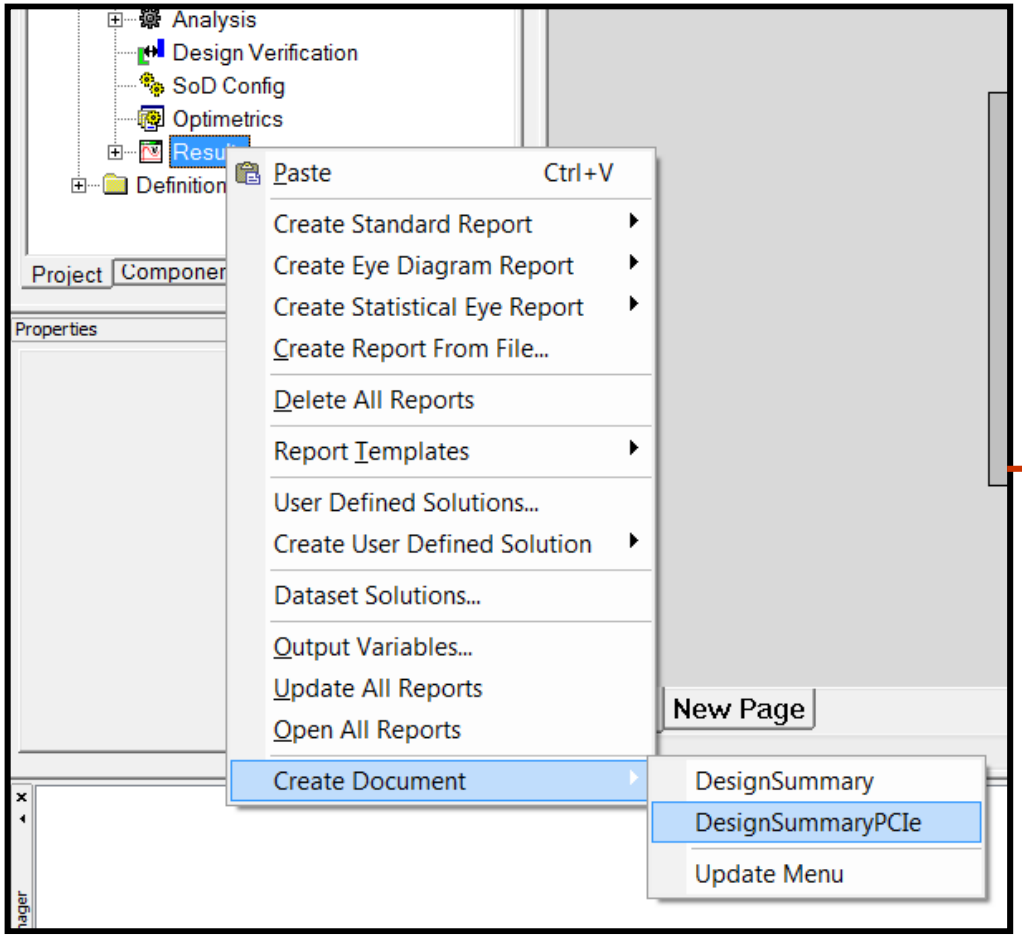


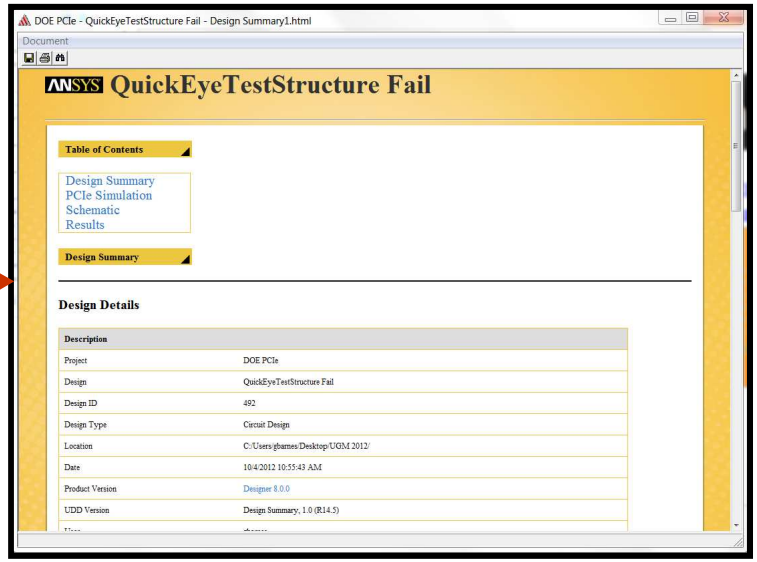
DesignerSI – Time Domain Specification



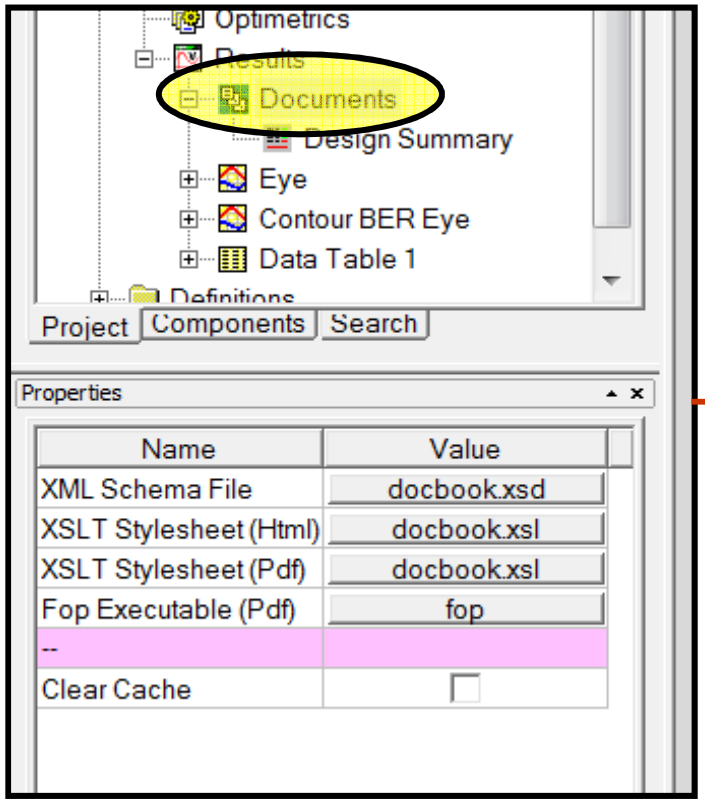


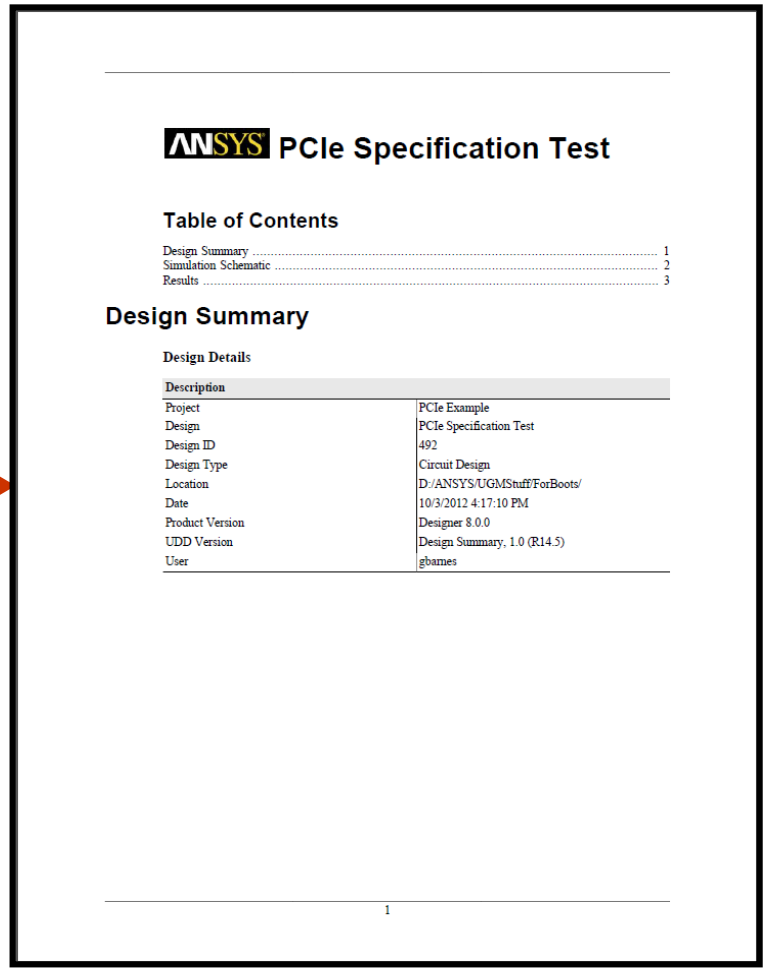
User Defined Document (UDD)





UDD





ANSYS PCIe Specification Test

Table of Contents

Design Summary

Design Details

Description	
Project	PCIe Example
Design	PCIe Specification Test
Design ID	492
Design Type	Circuit Design
Location	D:/ANSYS/UGMStuff/ForBoots/
Date	10/3/2012 4:17:10 PM
Product Version	Designer 8.0.0
UDD Version	Design Summary, 1.0 (R14.5)
User	gbarnes

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Summary

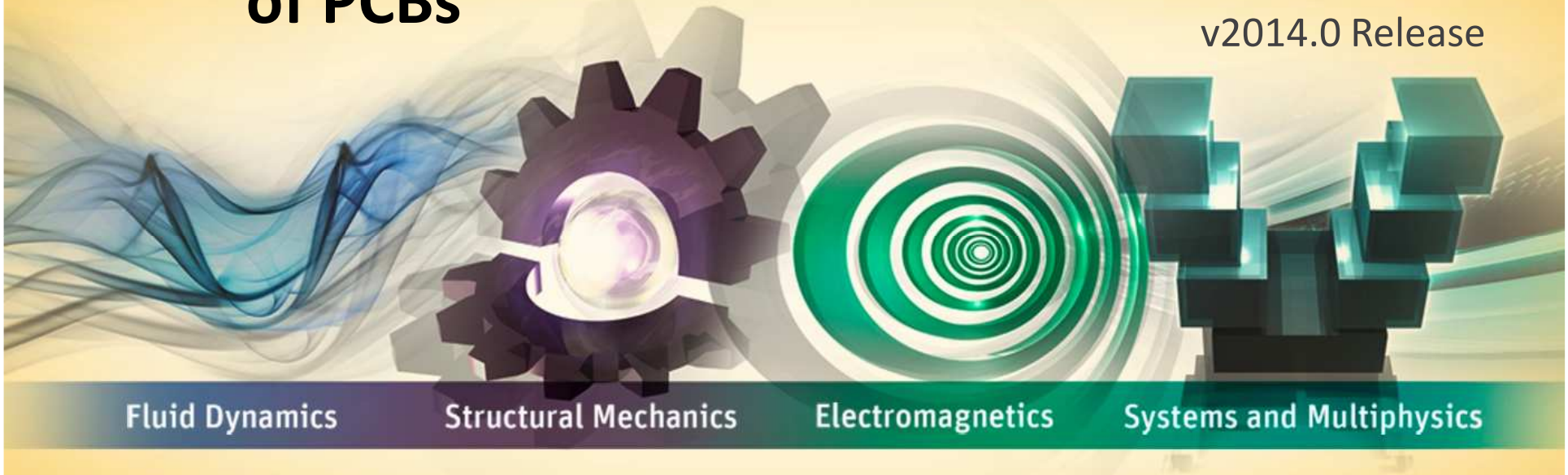
- **SIwave merged with Alinks to provide a very cohesive flow from import to simulation.**
- **SIwave has multiple solver technology options for the users needs.**
  - Power integrity and signal integrity
- **SIwave can be used solely as a front end tool or linked with DesignerSI to handle any type of post validation channel simulation.**
- **UDO and UDD within Designer enable users to customize and easily create validation kits and report generation.**
- **The ANSYS post validation solution backed with accurate electromagnetic models allows root cause trouble shooting and optimization.**

ANSYS

Realize Your Product Promise®

Modern Simulation Solutions for Signal and Power Integrity for Efficient Design of PCBs

v2014.0 Release



Peter Krenz, Application Engineer